

Model Name: ST4265-BI

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCI EXPRESS*16 SLOT
10	PCH_FDI,DMI,USB,PCIE
11	PCH_DP,CLK BUFFER
12	PCH_HOST,SATA,PCI
13	PCH_GPIO,CTRL,AUDIO
14	PCH_PWR,GND
15	PCH_HDMI,DVI,DP
16	PCI EXPRESS*4 SLOT
17	PCI & PCIEX1 SLOT
18	LAN_RTL8111DP
19	ITE 8728 LPC IO
20	COM,LPT
21	BIOS, TPM
22	VCORE /VAXG PWM_ISL95836-1
23	VCORE /VAXG PWM_ISL95836-2
24	RT8120-DDR POWWER
25	RT8120-VTT POWER
26	DISCRET POWER1
27	DISCRET POWER2

SHEET

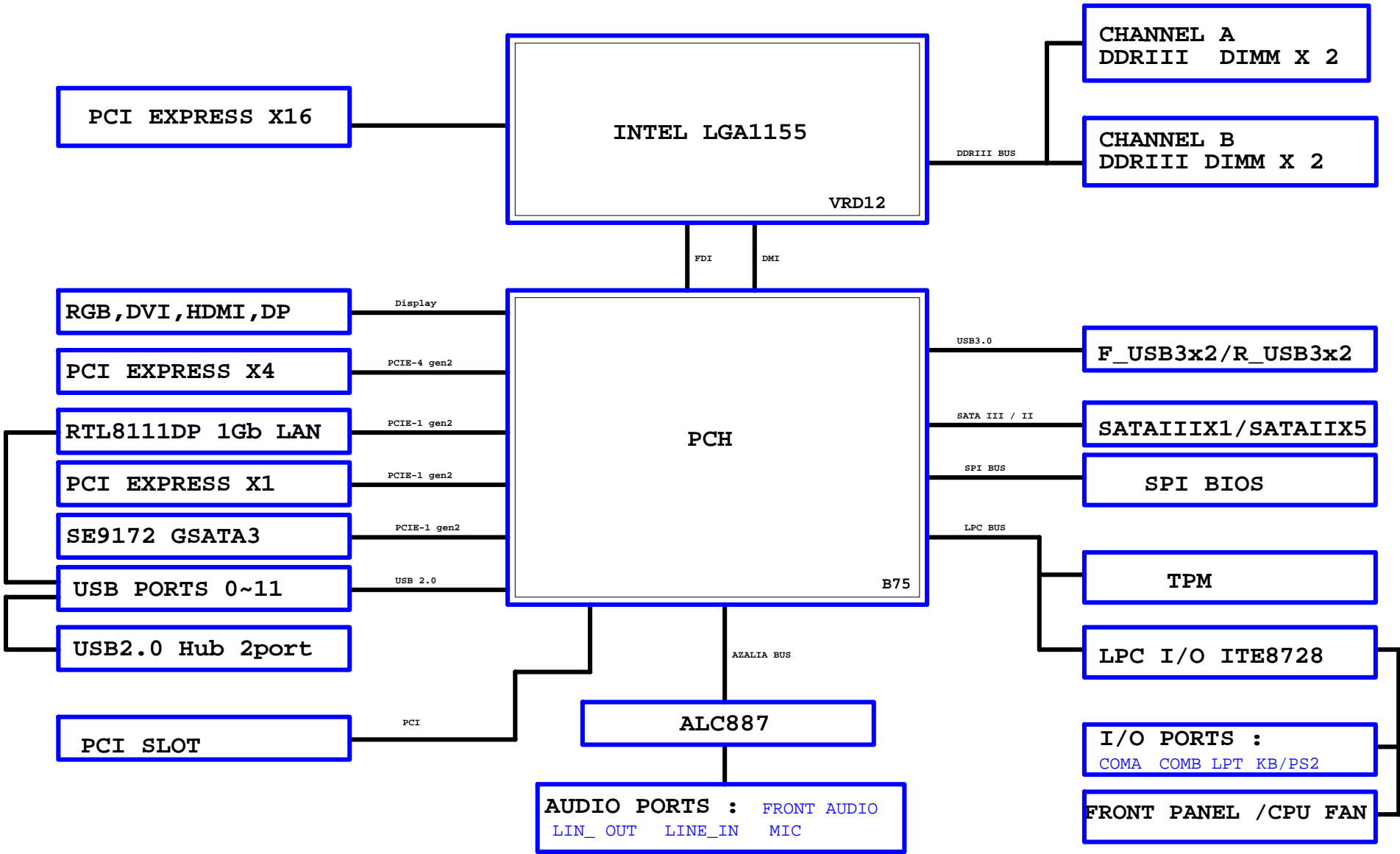
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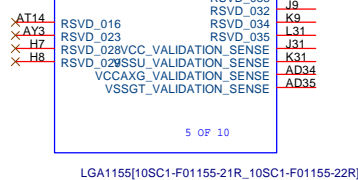
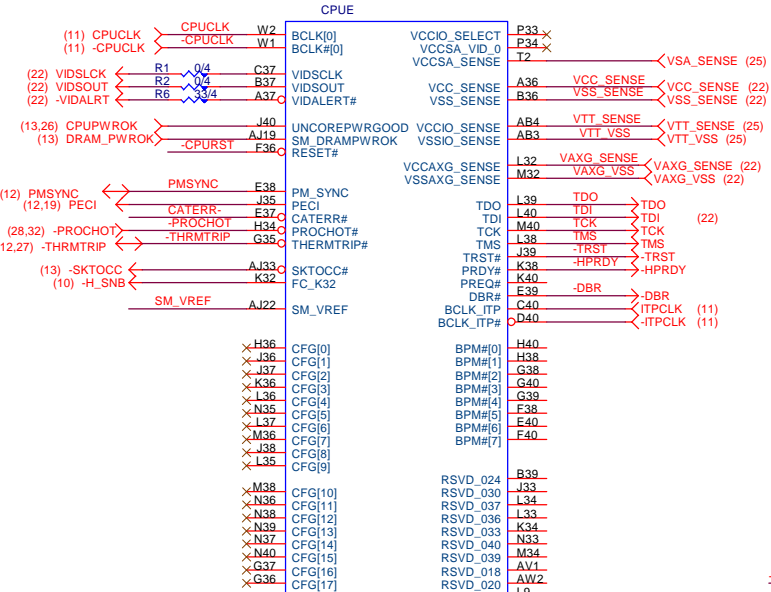
28	ATX,RUSB,PROCHOT-
29	AUDIO CODEC
30	REAR AUDIO JACK
31	FP,FUSB,SPKR
32	HWM,KB/MS, FAN CTRL
33	M9172-GSATA3
34	USB2.0 Hub uPD720114
35	
36	

GIGABYTE

Title		
Cover Sheet		
Size	Document Number	Rev
Custom	ST4265-BI	1.0
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BLOCK DIAGRAM

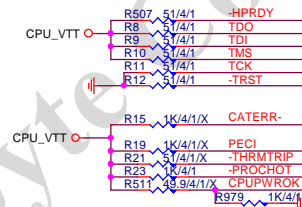
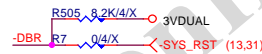
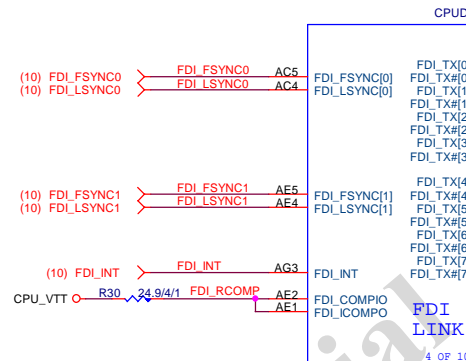
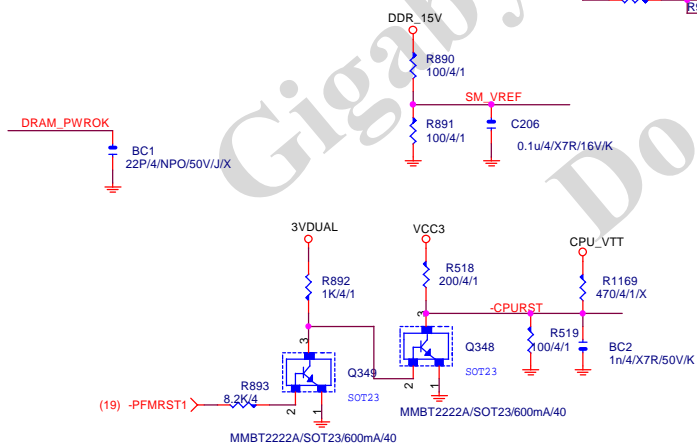




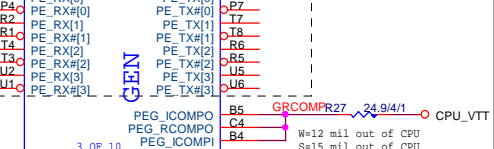
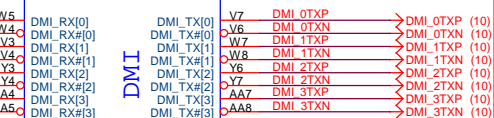
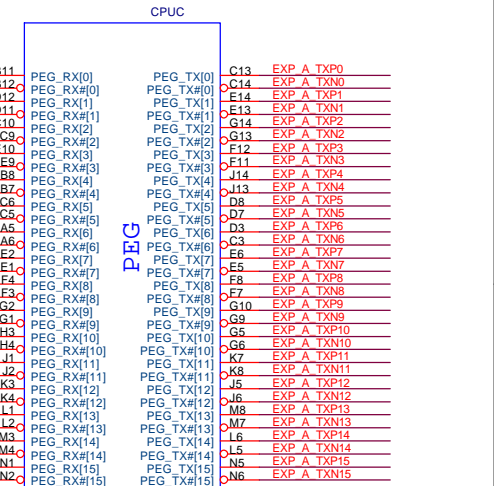
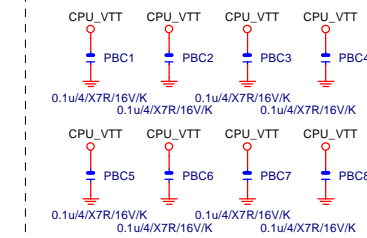
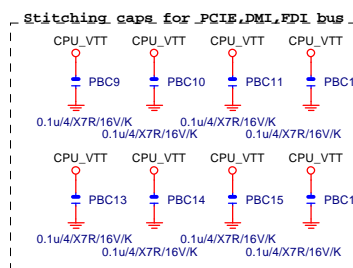
CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	RSVD	RSVD	RSVD
3	RSVD	RSVD	RSVD
4	RSVD	RSVD	RSVD
5	RSVD	RSVD	RSVD
6	RSVD	RSVD	RSVD
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIE CONFIG
1	1	1X16, Default
1	0	2X8
0	1	RSVD
0	0	X8_X4_X4

CFG 0-17 all internal PULL-UP



-Prochot pu change to 1K from 51 ,for the PWM IC sink level must under 0.3VTT when drive Low.



LGA1155[10SC1-F01155-21R_10SC1-F01155-22R]			
Title			
CPU LGA1155-A			
Size	Document Number	Rev	
Cuspm	ST4265-BI	1.0	
Date:	Wednesday, May 30, 2012	Sheet 4 of 34	

CPUA

MAAA0	AV27	SA_MA[0]	SA_DQS[0]	AK3	DQSA0
MAAA1	AY24	SA_MA[1]	SA_DQS[0]	AK2	-DQSA0
MAAA2	AW24	SA_MA[2]			
MAAA3	AW23	SA_MA[3]			
MAAA4	AV23	SA_MA[4]	SA_DQ[0]	AJ3	MDA0
MAAA5	AT24	SA_MA[5]	SA_DQ[1]	AJ4	MDA1
MAAA6	AT23	SA_MA[6]	SA_DQ[2]	AL3	MDA2
MAAA7	AU22	SA_MA[7]	SA_DQ[3]	AL4	MDA3
MAAA8	AV22	SA_MA[8]	SA_DQ[4]	AJ2	MDA4
MAAA9	AT22	SA_MA[9]	SA_DQ[5]	AJ1	MDA5
MAAA10	AV28	SA_MA[10]	SA_DQ[6]	AL2	MDA6
MAAA11	AU21	SA_MA[11]	SA_DQ[7]	AL1	MDA7
MAAA12	AT21	SA_MA[12]			
MAAA13	AW32	SA_MA[13]	SA_DQS[1]	AP3	DQSA1
MAAA14	AU20	SA_MA[14]	SA_DQS[1]	AP2	-DQSA1
MAAA15	AT20	SA_MA[15]			
(7) -SWEA	AW29	SA_WE#	SA_DQ[8]	AN1	MDA8
(7) -SCASA	AV30	SA_CAS#	SA_DQ[9]	AN4	MDA9
(7) -SRASA	AU28	SA_RAS#	SA_DQ[10]	AR3	MDA10
(7) SBAA0	AY29	SA_BS[0]	SA_DQ[11]	AR4	MDA12
(7) SBAA1	AW28	SA_BS[1]	SA_DQ[12]	AN2	MDA11
(7) SBAA2	AV20	SA_BS[2]	SA_DQ[13]	AN3	MDA13
(7) -CSA0	AU29	SA_CS#	SA_DQ[14]	AR2	MDA14
(7) -CSA1	AV32	SA_CS#	SA_DQ[15]	AR1	MDA15
(7) -CSA2	AW30	SA_CS#	SA_DQS[2]	AW4	DQSA2
(7) -CSA3	AU33	SA_CS#	SA_DQS[2]	AW4	-DQSA2
(7) CKEA0	AV19	SA_CKE[0]	SA_DQ[16]	AV2	MDA16
(7) CKEA1	AT19	SA_CKE[1]	SA_DQ[17]	AW3	MDA17
(7) CKEA2	AU18	SA_CKE[2]	SA_DQ[18]	AV5	MDA18
(7) CKEA3	AV18	SA_CKE[3]	SA_DQ[19]	AW5	MDA19
MODT_A0	AV31	SA_ODT[0]	SA_DQ[20]	AU2	MDA20
MODT_A1	AU32	SA_ODT[1]	SA_DQ[21]	AU3	MDA21
MODT_A2	AU30	SA_ODT[2]	SA_DQ[22]	AU5	MDA22
MODT_A3	AW33	SA_ODT[3]	SA_DQ[23]	AY5	MDA23
(7) DCLKA0	AY25	SA_CK[0]	SA_DQS[3]	AV8	DQSA3
(7) -DCLKA0	AW25	SA_CK[0]	SA_DQS[3]	AW8	-DQSA3
(7) DCLKA1	AU24	SA_CK[1]			
(7) -DCLKA1	AU25	SA_CK[1]	SA_DQ[24]	AY7	MDA24
(7) DCLKA2	AW27	SA_CK[2]	SA_DQ[25]	AU7	MDA25
(7) -DCLKA2	AY27	SA_CK[2]	SA_DQ[26]	AV9	MDA26
(7) DCLKA3	AW26	SA_CK[3]	SA_DQ[27]	AU9	MDA27
(7) -DCLKA3	AV26	SA_CK[3]	SA_DQ[28]	AV7	MDA28
(7) DCLKA0	AY25	SA_CK[0]	SA_DQ[29]	AW7	MDA29
(7) -DCLKA0	AW25	SA_CK[0]	SA_DQ[30]	AW9	MDA30
(7) DCLKA1	AU24	SA_CK[1]	SA_DQ[31]	AY9	MDA31
(7) -DCLKA1	AU25	SA_CK[1]			
(7) DCLKA2	AW27	SA_CK[2]	SA_DQS[4]	AV37	DQSA4
(7) -DCLKA2	AY27	SA_CK[2]	SA_DQS[4]	AV36	-DQSA4
(7) DCLKA3	AW26	SA_CK[3]			
(7) -DCLKA3	AV26	SA_CK[3]	SA_DQ[32]	AU35	MDA32
(7) DCLKA0	AY25	SA_CK[0]	SA_DQ[33]	AW37	MDA33
(7) -DCLKA0	AW25	SA_CK[0]	SA_DQ[34]	AU39	MDA34
(7) DCLKA1	AU24	SA_CK[1]	SA_DQ[35]	AU36	MDA35
(7) -DCLKA1	AU25	SA_CK[1]	SA_DQ[36]	AW35	MDA36
(7) DCLKA2	AW27	SA_CK[2]	SA_DQ[37]	AY36	MDA37
(7) -DCLKA2	AY27	SA_CK[2]	SA_DQ[38]	AU38	MDA38
(7) DCLKA3	AW26	SA_CK[3]	SA_DQ[39]	AU37	MDA39
(7) -DCLKA3	AV26	SA_CK[3]			
(7) DCLKA0	AY25	SA_CK[0]	SA_DQS[5]	AP38	DQSA5
(7) -DCLKA0	AW25	SA_CK[0]	SA_DQS[5]	AP39	-DQSA5
(7) DCLKA1	AU24	SA_CK[1]			
(7) -DCLKA1	AU25	SA_CK[1]	SA_DQ[40]	AR40	MDA40
(7) DCLKA2	AW27	SA_CK[2]	SA_DQ[41]	AR37	MDA41
(7) -DCLKA2	AY27	SA_CK[2]	SA_DQ[42]	AN38	MDA42
(7) DCLKA3	AW26	SA_CK[3]	SA_DQ[43]	AN37	MDA43
(7) -DCLKA3	AV26	SA_CK[3]	SA_DQ[44]	AR39	MDA44
(7) DCLKA0	AY25	SA_CK[0]	SA_DQ[45]	AR38	MDA45
(7) -DCLKA0	AW25	SA_CK[0]	SA_DQ[46]	AN39	MDA46
(7) DCLKA1	AU24	SA_CK[1]	SA_DQ[47]	AN40	MDA47
(7) -DCLKA1	AU25	SA_CK[1]			
(7) DCLKA2	AW27	SA_CK[2]	SA_DQS[6]	AK38	DQSA6
(7) -DCLKA2	AY27	SA_CK[2]	SA_DQS[6]	AK39	-DQSA6
(7) DCLKA3	AW26	SA_CK[3]			
(7) -DCLKA3	AV26	SA_CK[3]	SA_DQ[48]	AL40	MDA48
(7) DCLKA0	AY25	SA_CK[0]	SA_DQ[49]	AL37	MDA49
(7) -DCLKA0	AW25	SA_CK[0]	SA_DQ[50]	AJ38	MDA50
(7) DCLKA1	AU24	SA_CK[1]	SA_DQ[51]	AJ37	MDA51
(7) -DCLKA1	AU25	SA_CK[1]	SA_DQ[52]	AL39	MDA52
(7) DCLKA2	AW27	SA_CK[2]	SA_DQ[53]	AL38	MDA53
(7) -DCLKA2	AY27	SA_CK[2]	SA_DQ[54]	AJ39	MDA54
(7) DCLKA3	AW26	SA_CK[3]	SA_DQ[55]	AJ40	MDA55
(7) -DCLKA3	AV26	SA_CK[3]			
(7) DCLKA0	AY25	SA_CK[0]	SA_DQS[7]	AF38	DQSA7
(7) -DCLKA0	AW25	SA_CK[0]	SA_DQS[7]	AF39	-DQSA7
(7) DCLKA1	AU24	SA_CK[1]			
(7) -DCLKA1	AU25	SA_CK[1]	SA_DQ[56]	AG40	MDA56
(7) DCLKA2	AW27	SA_CK[2]	SA_DQ[57]	AG37	MDA57
(7) -DCLKA2	AY27	SA_CK[2]	SA_DQ[58]	AE38	MDA58
(7) DCLKA3	AW26	SA_CK[3]	SA_DQ[59]	AE37	MDA59
(7) -DCLKA3	AV26	SA_CK[3]	SA_DQ[60]	AG39	MDA60
(7) DCLKA0	AY25	SA_CK[0]	SA_DQ[61]	AG38	MDA61
(7) -DCLKA0	AW25	SA_CK[0]	SA_DQ[62]	AE39	MDA62
(7) DCLKA1	AU24	SA_CK[1]	SA_DQ[63]	AE40	MDA63
(7) -DCLKA1	AU25	SA_CK[1]			

DDR_0

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LGA1155[10SC1-F01155-21R_10SC1-F01155-22R]

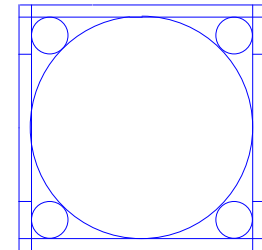
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MAAB2	AM19	SB_MA[2]			
MAAB3	AK18	SB_MA[3]			
MAAB4	AP19	SB_MA[4]	SB_DQ[0]	AG7	MDB0
MAAB5	AP18	SB_MA[5]	SB_DQ[1]	AG8	MDB1
MAAB6	AM18	SB_MA[6]	SB_DQ[2]	AJ9	MDB2
MAAB7	AL18	SB_MA[7]	SB_DQ[3]	AJ8	MDB3
MAAB8	AY17	SB_MA[8]	SB_DQ[4]	AG8	MDB4
MAAB9	AY17	SB_MA[9]	SB_DQ[5]	AG8	MDB5
MAAB10	AN23	SB_MA[10]	SB_DQ[6]	AJ6	MDB6
MAAB11	AU17	SB_MA[11]	SB_DQ[7]	AJ7	MDB7
MAAB12	AT18	SB_MA[12]			
MAAB13	AR26	SB_MA[13]	SB_DQS[1]	AM8	DQSB1
MAAB14	AY16	SB_MA[14]	SB_DQS[1]	AL8	-DQSB1
MAAB15	AV16	SB_MA[15]			
(8) -SWEB	AR25	SB_WE#	SB_DQ[8]	AL7	MDB8
(8) -SCASB	AK25	SB_CAS#	SB_DQ[9]	AM7	MDB9
(8) -SRASB	AP24	SB_RAS#	SB_DQ[10]	AM10	MDB10
(8) SBAB0	AP23	SB_BS[0]	SB_DQ[11]	AL6	MDB12
(8) SBAB1	AM26	SB_BS[1]	SB_DQ[12]	AL6	MDB13
(8) SBAB2	AW17	SB_BS[2]	SB_DQ[13]	AL9	MDB14
(8) -CSB0	AN25	SB_CS#	SB_DQ[14]	AM9	MDB15
(8) -CSB1	AN26	SB_CS#	SB_DQ[15]		
(8) -CSB2	AL25	SB_CS#	SB_DQS[2]	AR8	DQSB2
(8) -CSB3	AT26	SB_CS#	SB_DQS[2]	AP8	-DQSB2
(8) CKEB0	AU16	SB_CKE[0]	SB_DQ[16]	AF7	MDB16
(8) CKEB1	AY15	SB_CKE[1]	SB_DQ[17]	AR7	MDB17
(8) CKEB2	AW15	SB_CKE[2]	SB_DQ[18]	AP10	MDB18
(8) CKEB3	AV15	SB_CKE[3]	SB_DQ[19]	AR10	MDB19
MODT_B0	AL26	SB_ODT[0]	SB_DQ[20]	AP6	MDB20
MODT_B1	AP26	SB_ODT[1]	SB_DQ[21]	AR6	MDB21
MODT_B2	AM26	SB_ODT[2]	SB_DQ[22]	AP9	MDB22
MODT_B3	AK26	SB_ODT[3]	SB_DQ[23]	AR9	MDB23
(8) DCLKB0	AL21	SB_CK[0]	SB_DQS[3]	AN13	DQSB3
(8) -DCLKB0	AL22	SB_CK[0]	SB_DQS[3]	AN12	-DQSB3
(8) DCLKB1	AK20	SB_CK[1]	SB_DQ[24]	AM12	MDB24
(8) -DCLKB1	AK20	SB_CK[1]	SB_DQ[25]	AM13	MDB25
(8) DCLKB2	AL23	SB_CK[2]	SB_DQ[26]	AR13	MDB26
(8) -DCLKB2	AL23	SB_CK[2]	SB_DQ[27]	AP13	MDB27
(8) DCLKB3	AP21	SB_CK[3]	SB_DQ[28]	AL12	MDB28
(8) -DCLKB3	AN21	SB_CK[3]	SB_DQ[29]	AL13	MDB29
(8) DCLKB0	AL21	SB_CK[0]	SB_DQ[30]	AR12	MDB30
(8) -DCLKB0	AL22	SB_CK[0]	SB_DQ[31]	AP12	MDB31
(8) DCLKB1	AK20	SB_CK[1]			
(8) -DCLKB1	AK20	SB_CK[1]	SB_DQS[4]	AN29	DQSB4
(8) DCLKB2	AL23	SB_CK[2]	SB_DQS[4]	AN28	-DQSB4
(8) -DCLKB2	AL23	SB_CK[2]	SB_DQ[32]	AR28	MDB32
(8) DCLKB3	AP21	SB_CK[3]	SB_DQ[33]	AR29	MDB33
(8) -DCLKB3	AN21	SB_CK[3]	SB_DQ[34]	AL28	MDB34
(8) DCLKB0	AL21	SB_CK[0]	SB_DQ[35]	AL29	MDB35
(8) -DCLKB0	AL22	SB_CK[0]	SB_DQ[36]	AP28	MDB36
(8) DCLKB1	AK20	SB_CK[1]	SB_DQ[37]	AP29	MDB37
(8) -DCLKB1	AK20	SB_CK[1]	SB_DQ[38]	AM28	MDB38
(8) DCLKB2	AL23	SB_CK[2]	SB_DQ[39]	AM29	MDB39
(8) -DCLKB2	AL23	SB_CK[2]			
(8) DCLKB3	AP21	SB_CK[3]	SB_DQS[5]	AP33	DQSB5
(8) -DCLKB3	AN21	SB_CK[3]	SB_DQS[5]	AR33	-DQSB5
(8) DCLKB0	AL21	SB_CK[0]			
(8) -DCLKB0	AL22	SB_CK[0]	SB_DQ[40]	AP32	MDB40
(8) DCLKB1	AK20	SB_CK[1]	SB_DQ[41]	AP31	MDB41
(8) -DCLKB1	AK20	SB_CK[1]	SB_DQ[42]	AP35	MDB42
(8) DCLKB2	AL23	SB_CK[2]	SB_DQ[43]	AP34	MDB43
(8) -DCLKB2	AL23	SB_CK[2]	SB_DQ[44]	AR32	MDB44
(8) DCLKB3	AP21	SB_CK[3]	SB_DQ[45]	AR31	MDB45
(8) -DCLKB3	AN21	SB_CK[3]	SB_DQ[46]	AR35	MDB46
(8) DCLKB0	AL21	SB_CK[0]	SB_DQ[47]	AR34	MDB47
(8) -DCLKB0	AL22	SB_CK[0]			
(8) DCLKB1	AK20	SB_CK[1]	SB_DQS[6]	AL33	DQSB6
(8) -DCLKB1	AK20	SB_CK[1]	SB_DQS[6]	AM33	-DQSB6
(8) DCLKB2	AL23	SB_CK[2]			
(8) -DCLKB2	AL23	SB_CK[2]	SB_DQ[48]	AM32	MDB48
(8) DCLKB3	AP21	SB_CK[3]	SB_DQ[49]	AM31	MDB49
(8) -DCLKB3	AN21	SB_CK[3]	SB_DQ[50]	AL35	MDB50
(8) DCLKB0	AL21	SB_CK[0]	SB_DQ[51]	AL32	MDB51
(8) -DCLKB0	AL22	SB_CK[0]	SB_DQ[52]	AM34	MDB52
(8) DCLKB1	AK20	SB_CK[1]	SB_DQ[53]	AL31	MDB53
(8) -DCLKB1	AK20	SB_CK[1]	SB_DQ[54]	AM35	MDB54
(8) DCLKB2	AL23	SB_CK[2]	SB_DQ[55]	AL34	MDB55
(8) -DCLKB2	AL23	SB_CK[2]			
(8) DCLKB3	AP21	SB_CK[3]	SB_DQS[7]	AG35	DQSB7
(8) -DCLKB3	AN21	SB_CK[3]	SB_DQS[7]	AG34	-DQSB7
(8) DCLKB0	AL21	SB_CK[0]			
(8) -DCLKB0	AL22	SB_CK[0]	SB_DQ[56]	AH35	MDB56
(8) DCLKB1	AK20	SB_CK[1]	SB_DQ[57]	AH34	MDB57
(8) -DCLKB1	AK20	SB_CK[1]	SB_DQ[58]	AE34	MDB58
(8) DCLKB2	AL23	SB_CK[2]	SB_DQ[59]	AE35	MDB59
(8) -DCLKB2	AL23	SB_CK[2]	SB_DQ[60]	AJ35	MDB60
(8) DCLKB3	AP21	SB_CK[3]	SB_DQ[61]	AJ34	MDB61
(8) -DCLKB3	AN21	SB_CK[3]	SB_DQ[62]	AF33	MDB62
(8) DCLKB0	AL21	SB_CK[0]	SB_DQ[63]	AF35	MDB63
(8) -DCLKB0	AL22	SB_CK[0]			

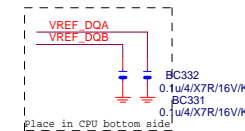
DDR_1

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LGA1155[10SC1-F01155-21R_10SC1-F01155-22R]

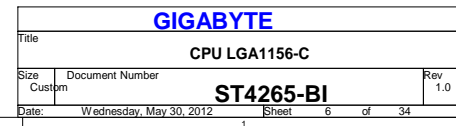
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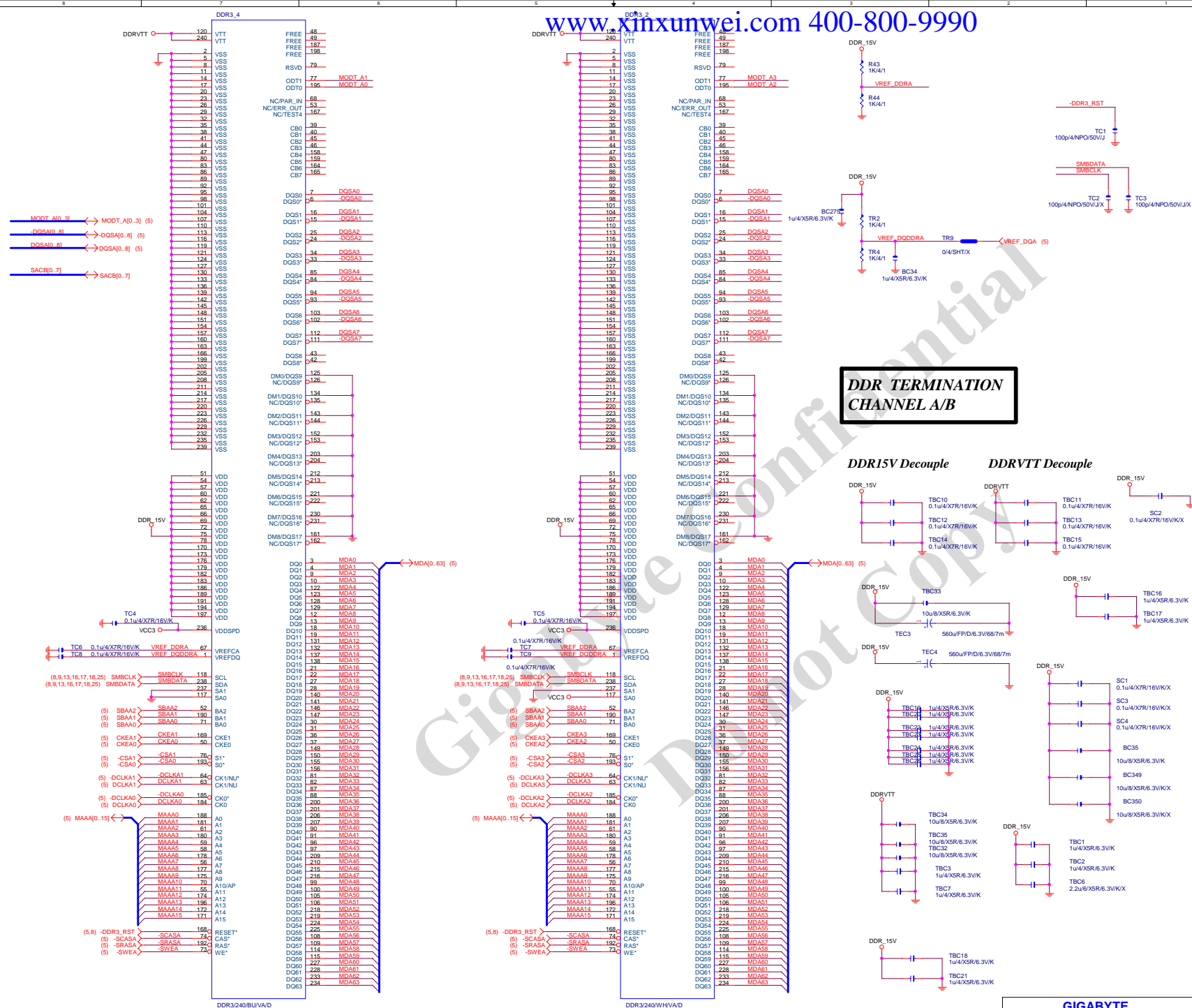
Need check the new CPU ME

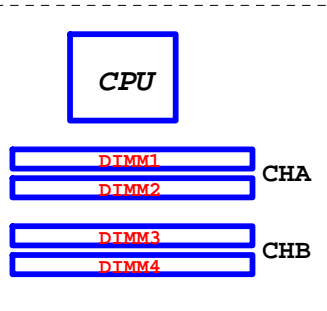


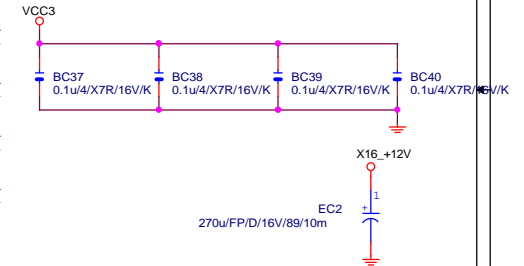
GIGABYTE

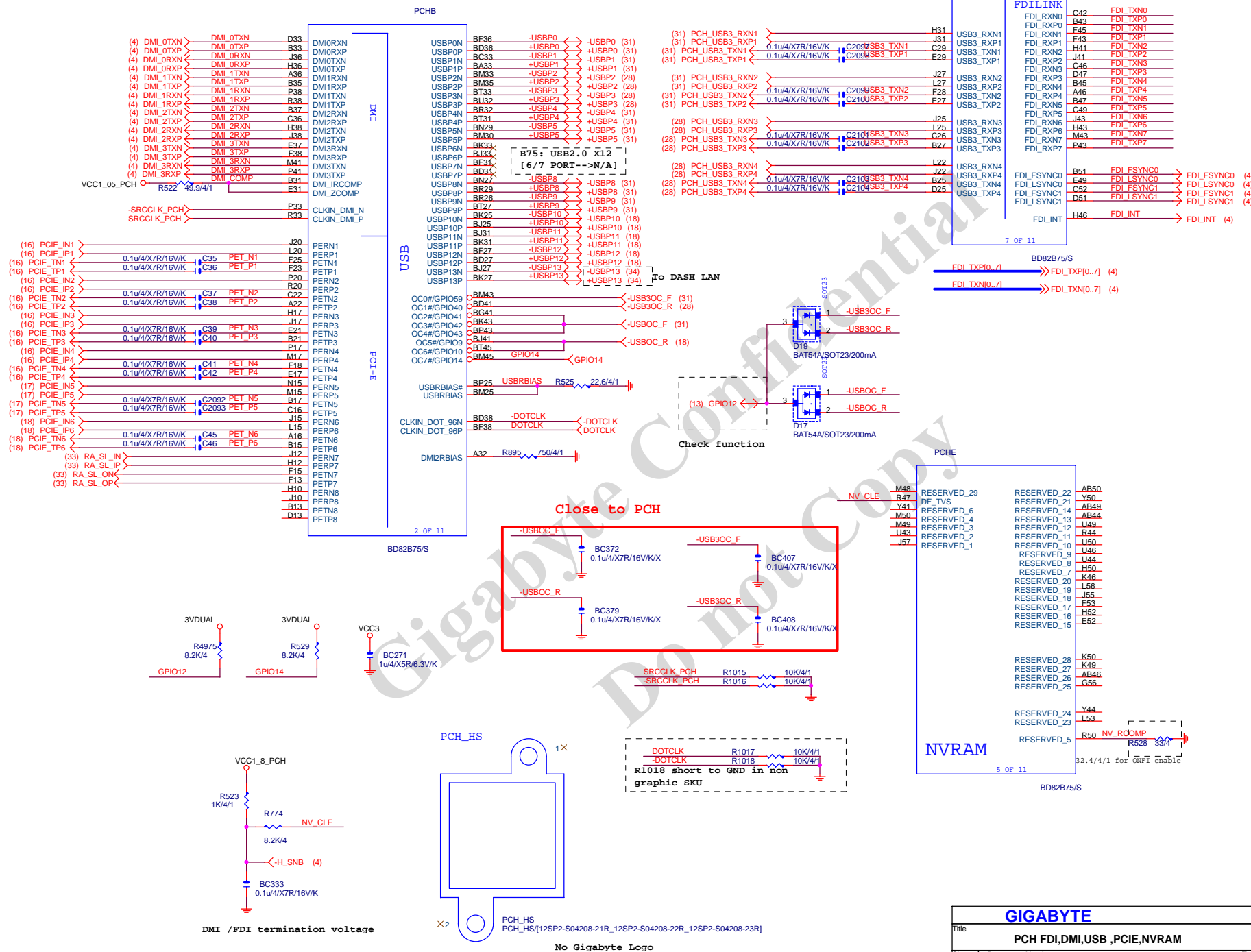
Title			CPU LGA1156-B		
Size			ST4265-BI		
Date:			Wednesday, May 30, 2012		
Sheet			5 of 34		

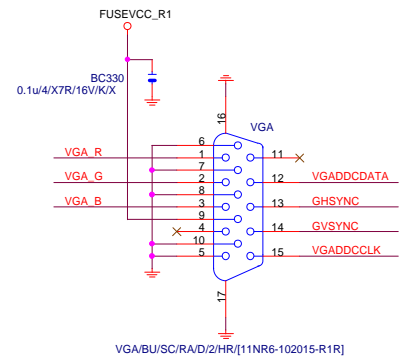
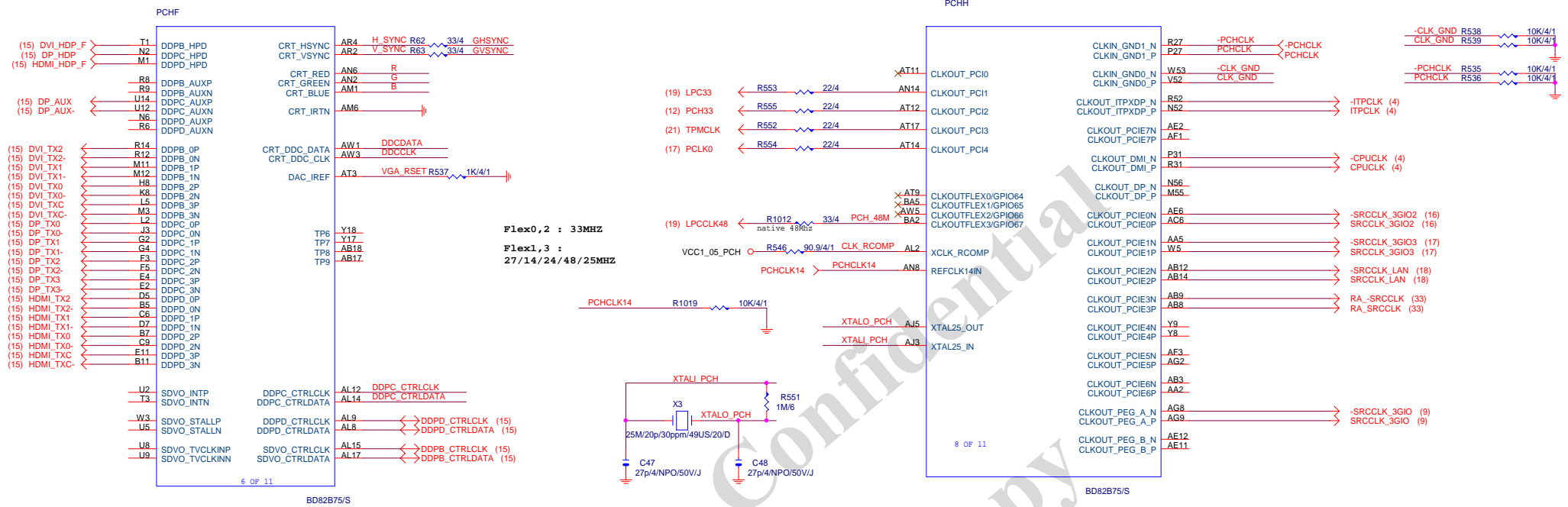




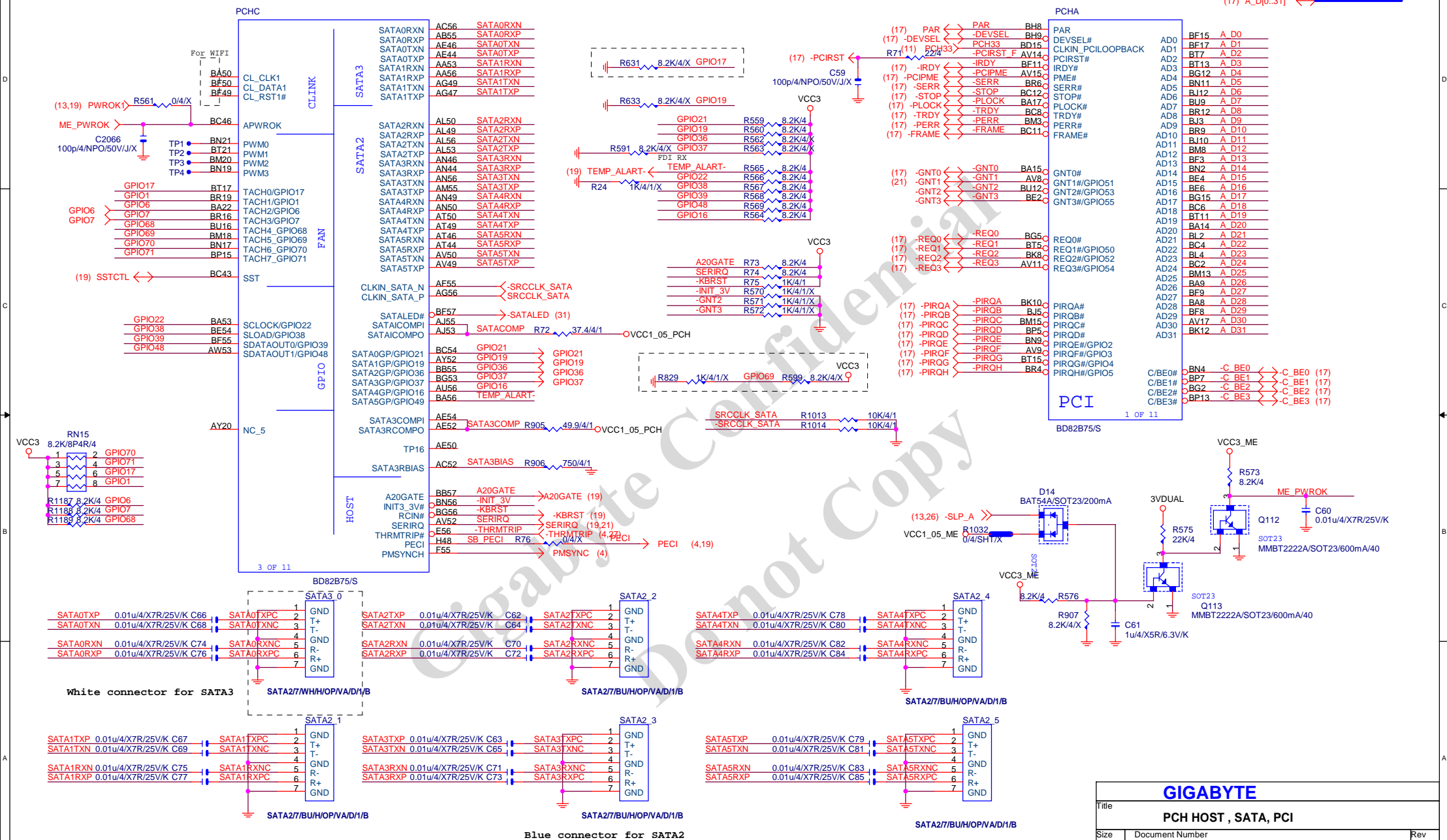


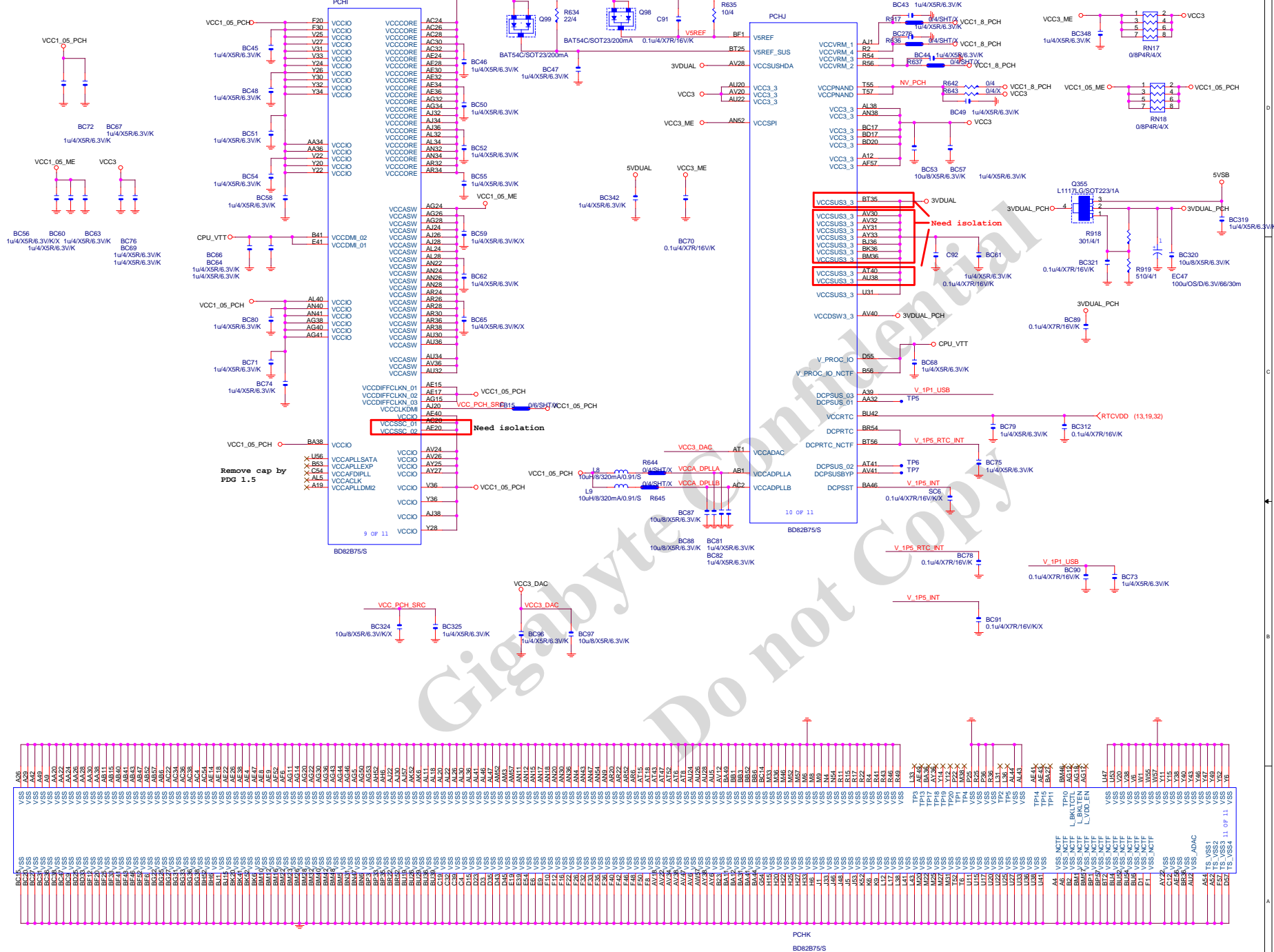


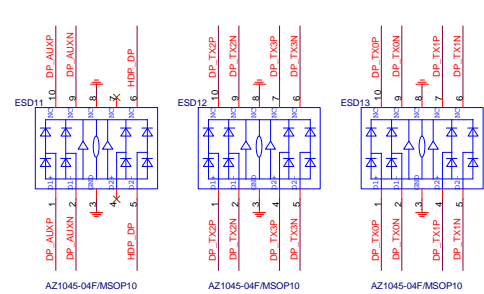
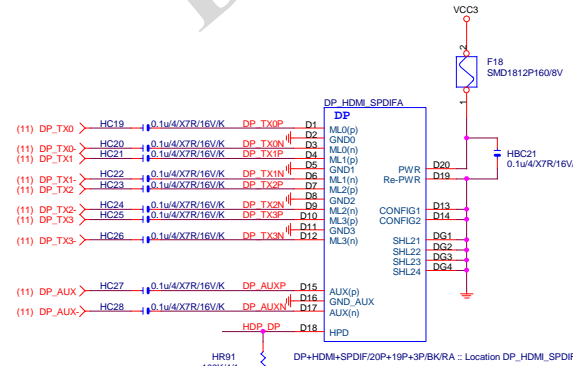
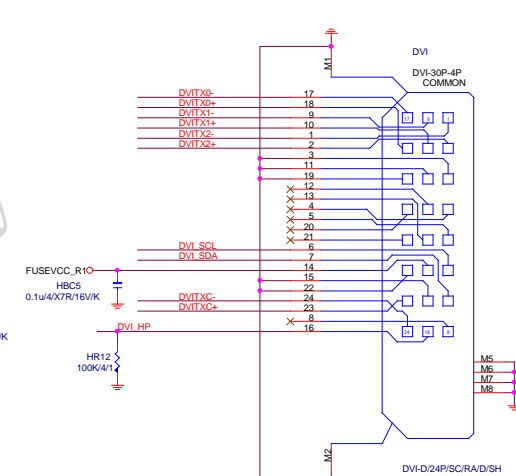
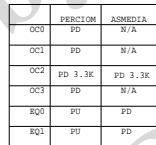
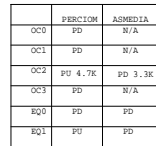
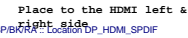


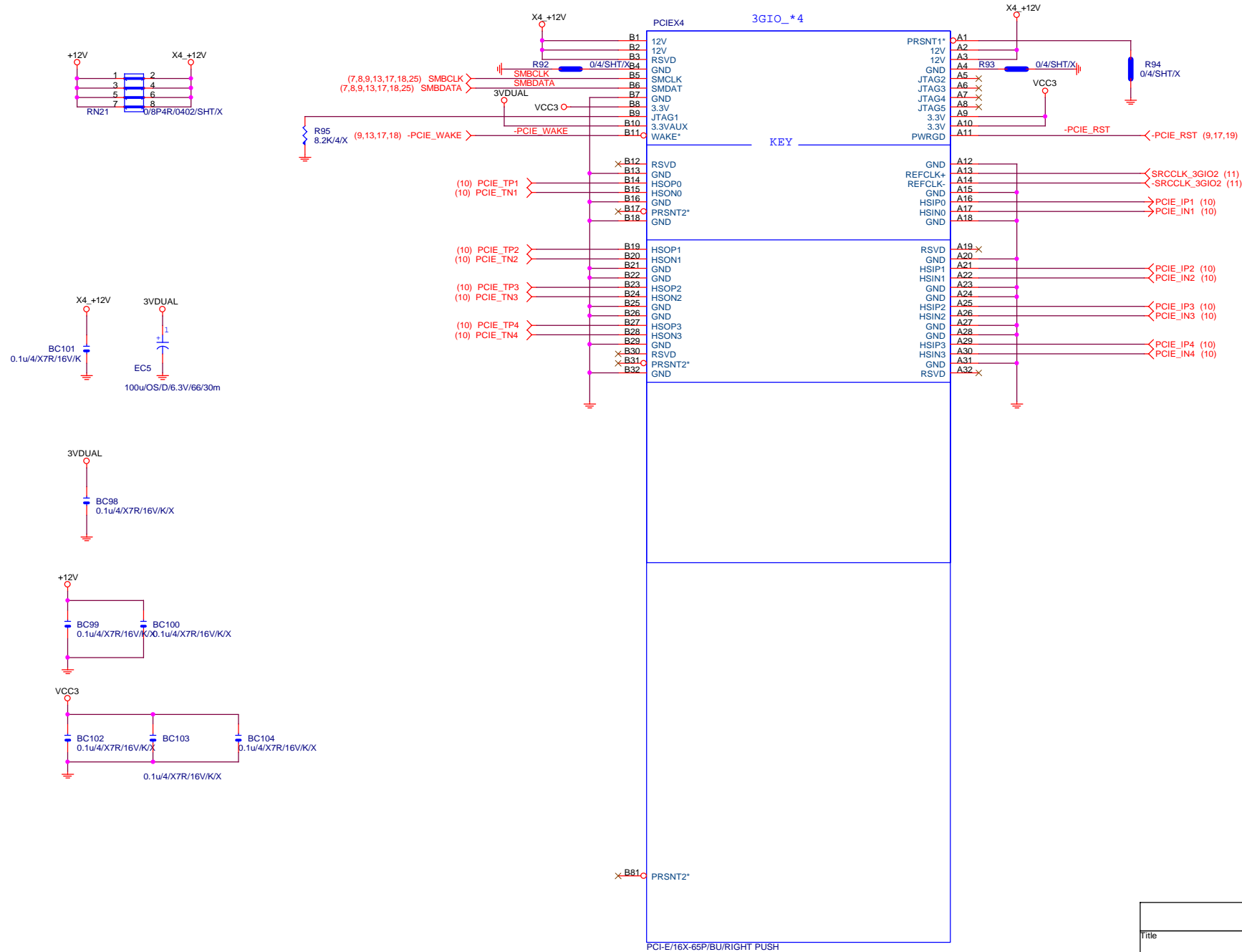


GIGABYTE			
PCH DISPLAY ,CLK BUFFER			
Title	Document Number	Rev	
Size	Custom	ST4265-BI	
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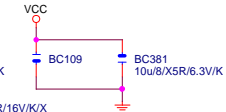
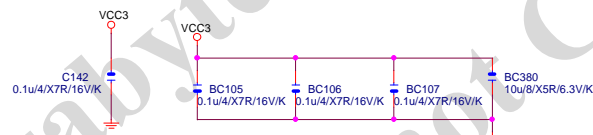




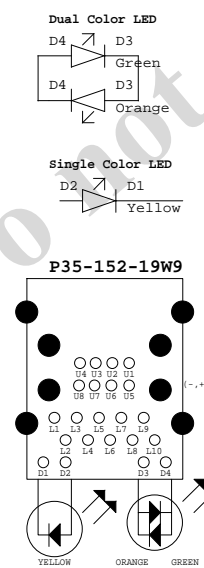
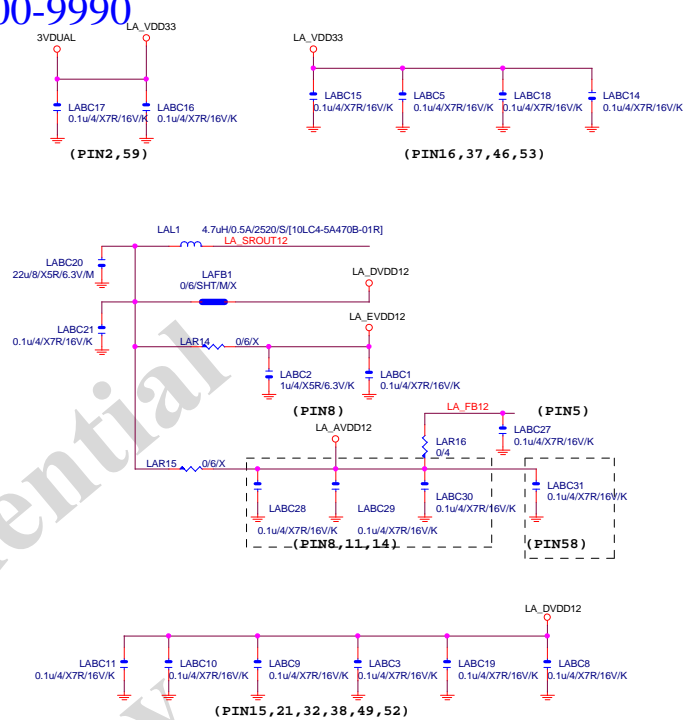


GIGABYTE

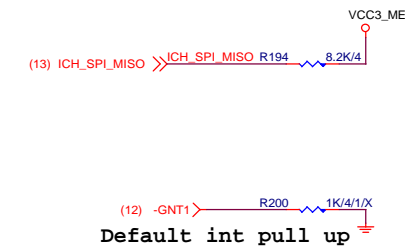
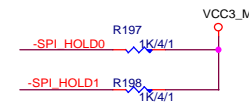
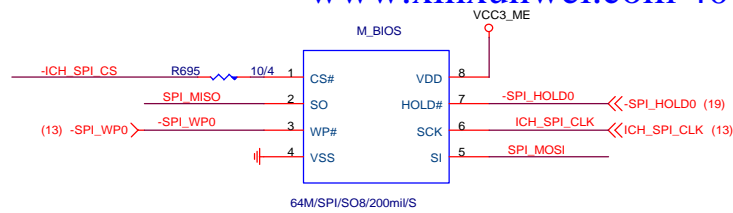
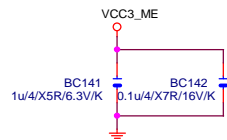
Title		
PCI EXPRESS X 4 PORT		
Size	Document Number	Rev
Custom	ST4265-BI	1.0
Date:	Wednesday, May 30, 2012	Sheet 16 of 34



Title			
PCIEX1,PCI SLOT			
Size Custom	Document Number		Rev
	ST4265-BI		1.0
Date:	Wednesday, May 30, 2012		Sheet 17 of 34

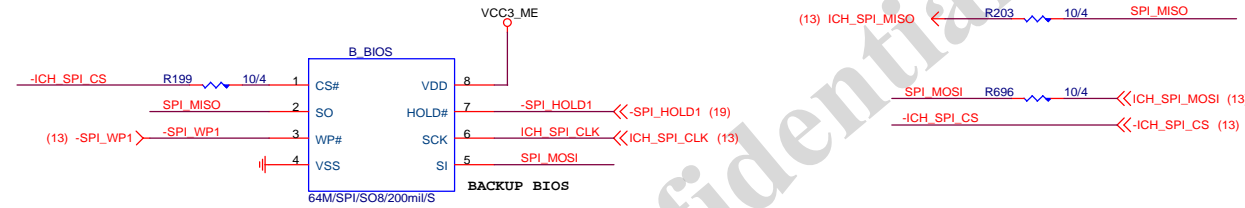






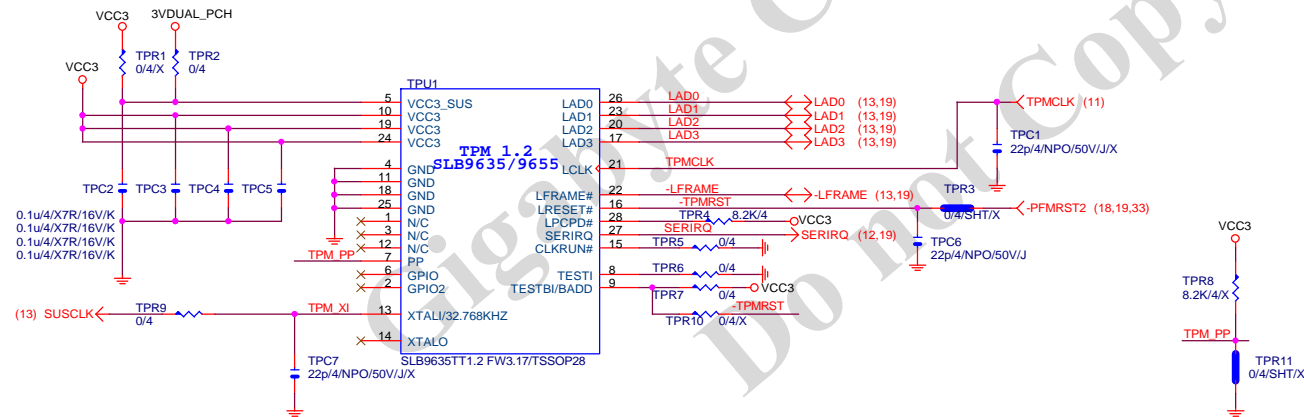
BOOT DEVICE	GNT1	GP19
LPC	0	0
PCI	1	0
SPI	1	1

1 means floating
0 means PD 1K



damp close to SPI flash

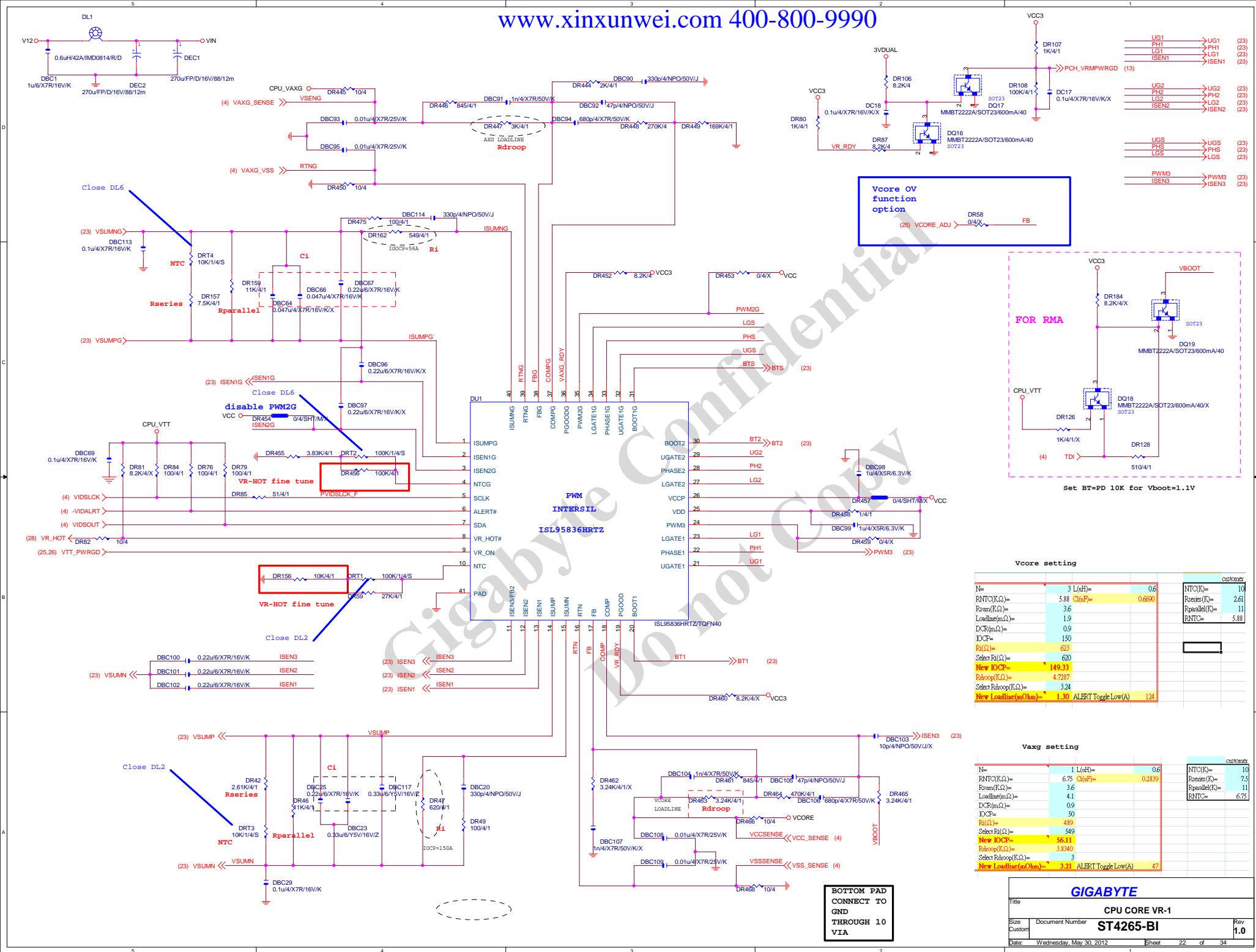
TPM



	SLB9635	SLB9655
TPR2, TPR4, TPR5, TPR6, TPR7, TPR9	MOUNT	N/A
TPR1, TPR10	N/A	MOUNT

GIGABYTE

Title			BIOS
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Voore setting			
N=	3	L(nH)=	0.6
RNTC(K Ω)=	5.88	Q(nP)=	0.6690
Fmns(K Ω)=	3.6		
Loadline(m Ω)=	1.9		
DCC(m Ω)=	0.9		
IOCP=	150		
Ri(Ω)=	623		
Select Ri(Ω)=	620		
New IOCP=	149.33		
Rdroop(K Ω)=	4.7287		
Select Rdroop(K Ω)=	3.24		
New Loadline(mOhm)=	1.30	ALERT Toggle Low(A)	124

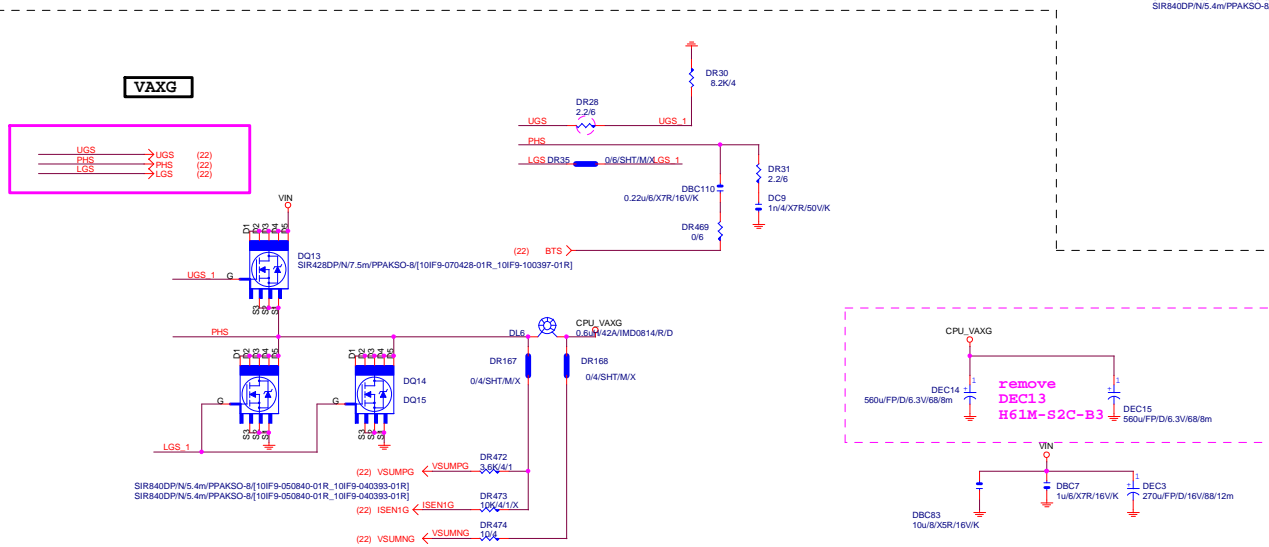
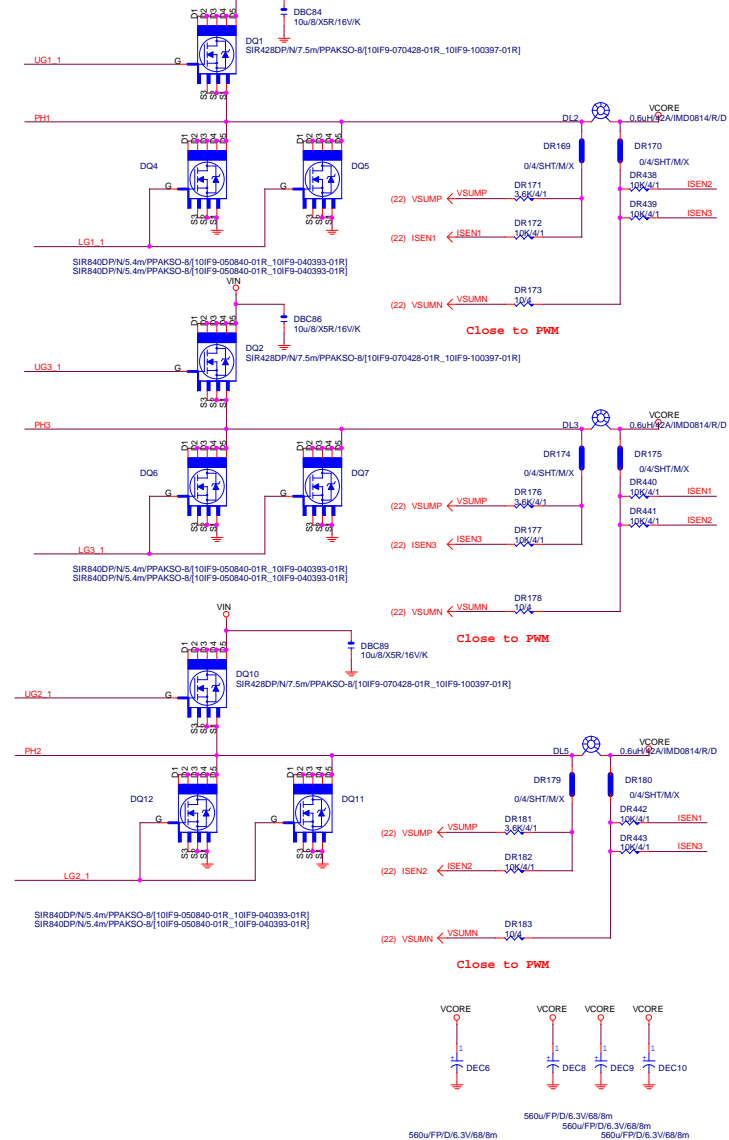
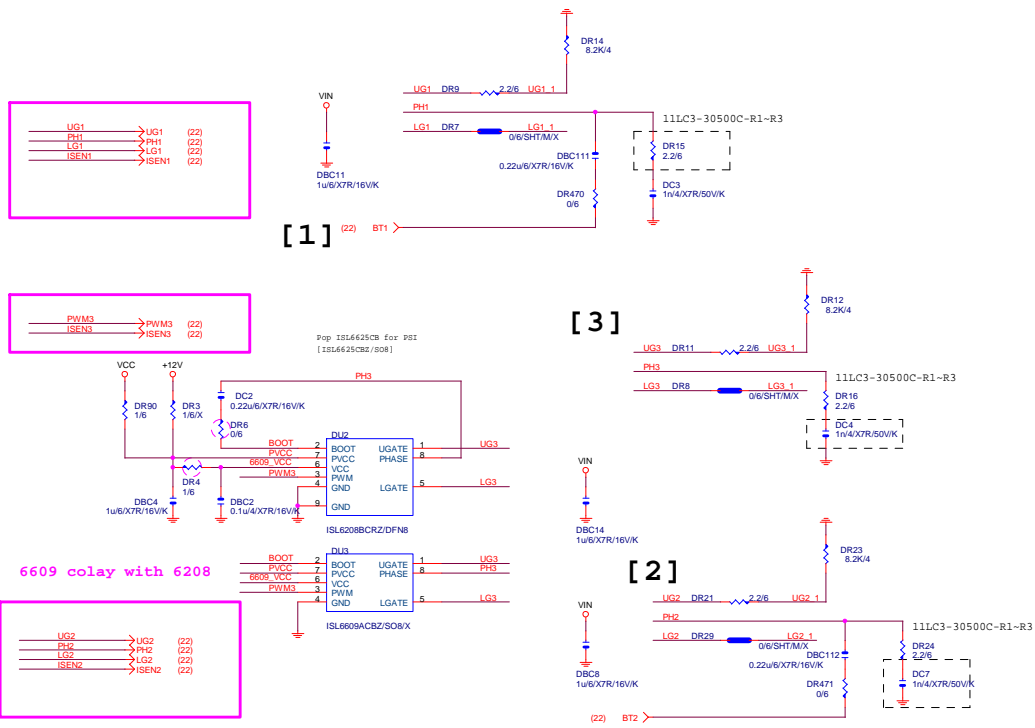
Vaux setting			Cost
N=	1 L(Off)	0.6	NTCH=
RNTC(KΩ)=	6.75 (OnP)	0.2839	Resistor (K)=
Form(KΩ)=	3.6		Equivalent(K)=
Loadline(mA)=	4.1		RNTC=
DRC(mΩ)=	0.9		
ICCP=	50		
Ri(Ω)=	489		
Select Ri(Ω)=	549		
New ICOP=	56.11		
Roboop(KΩ)=	3.8340		
Select Roboop(KΩ)=	3		
New Loadline(mA)=	3.21	ALERT Toggle Low(A)	47

GIGABYTE

Title	CPU CORE VR-
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Custom		

Date: Wednesday, May 30, 2012 Sheet 22 of 3



DDR_15V

OCP :
 $Rocset = (Iocp * Lgate, rdson) / Iocset$
 $Iocset = 10uA$

VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1
 IRMS=11.45A

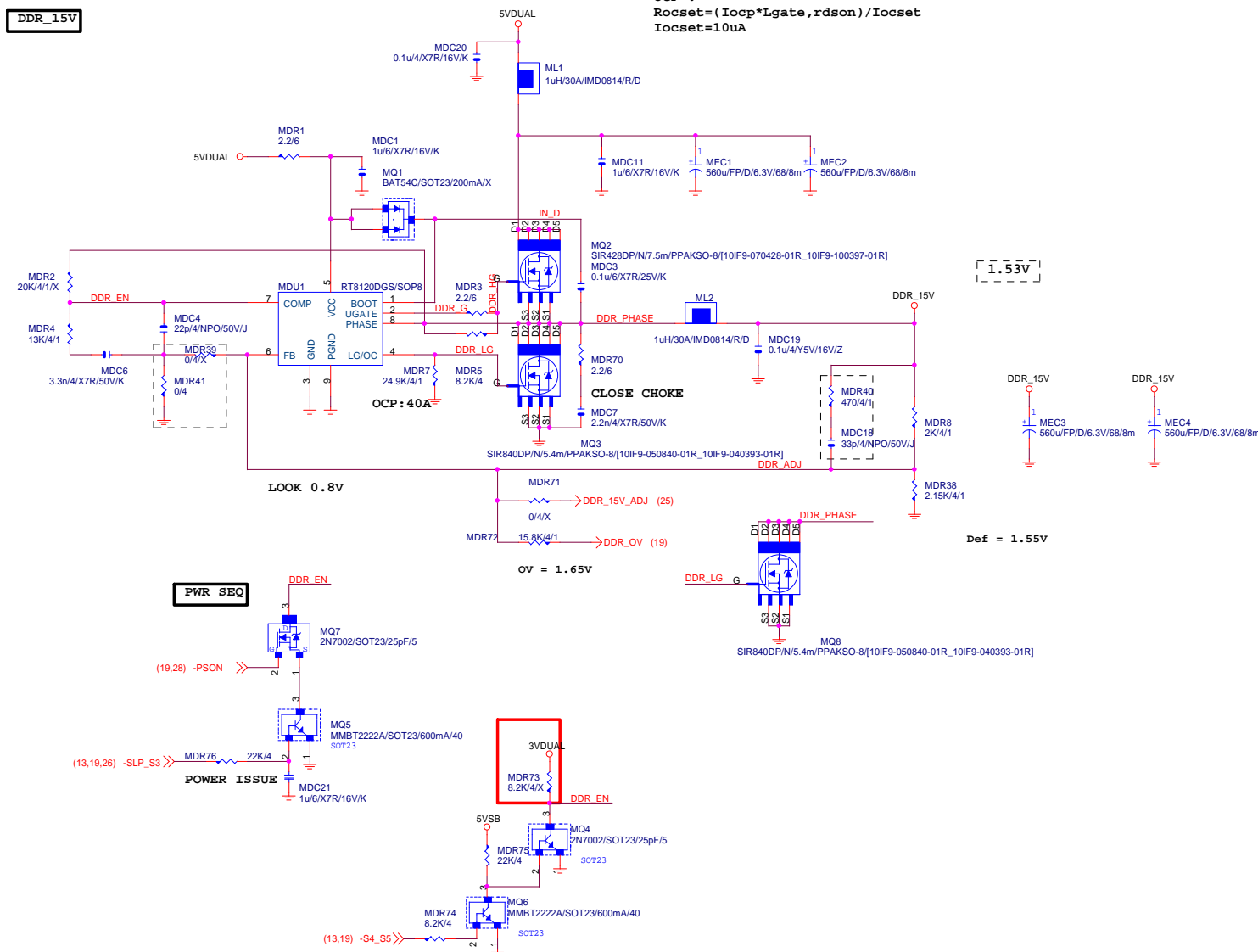
560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A
 Coefficient=1.7(85°C), 1(105°C)

VIN Ripple current=4.7X1.7=7.99A(85°C)

-->故固态电容须 $2X7.99=15.98 > 11.45A$

OCP : $Ipeak = (2 * Iocset * Rocset) / Rdson$
 typ Iocset=20uA , Rocset=4.7k

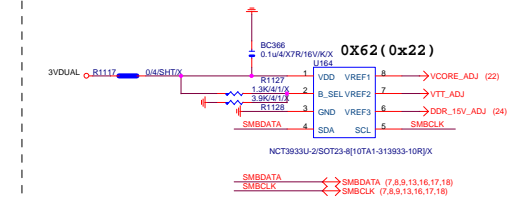
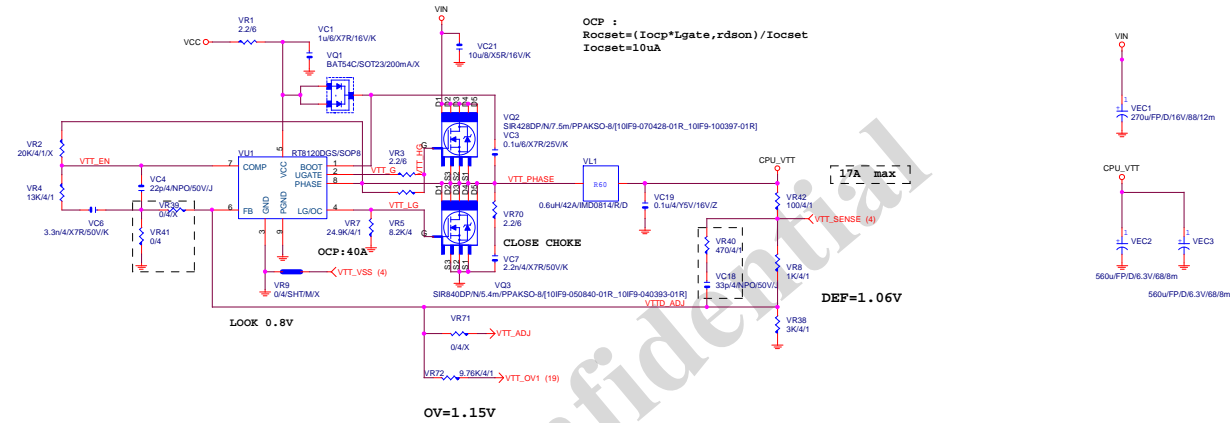
OCP : $53.71A = (2 * 20uA * 4.7k) / (7m / 7m)$



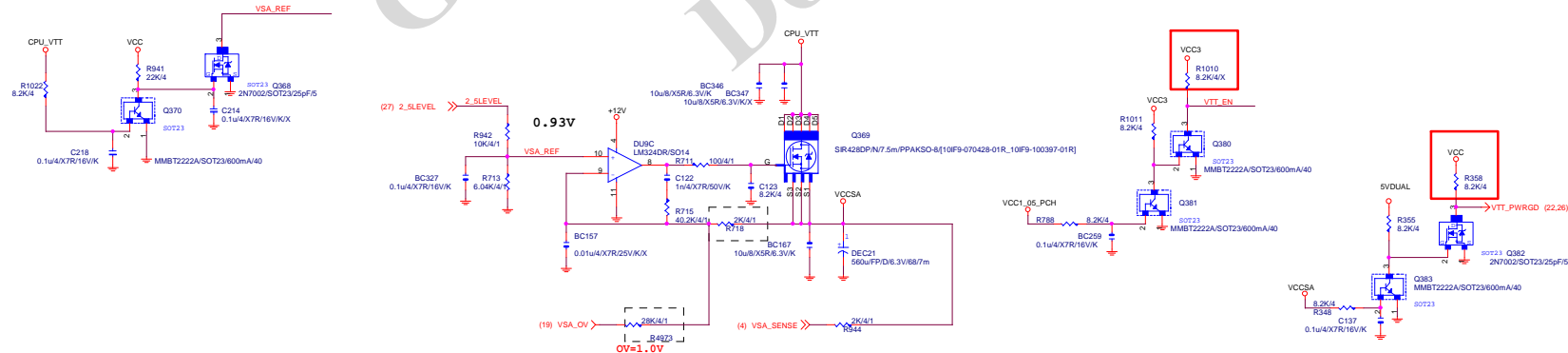
GIGABYTE

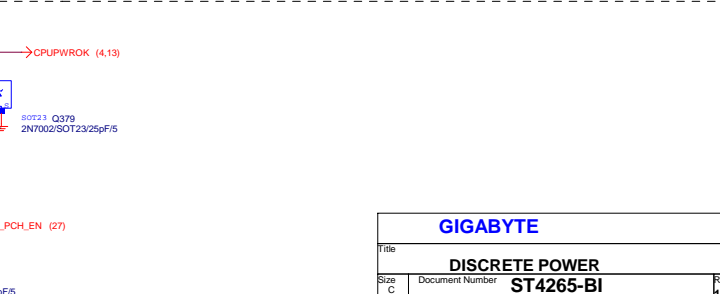
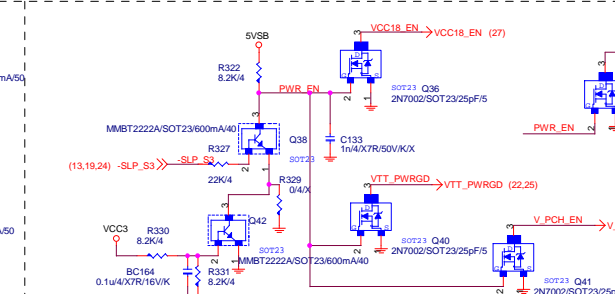
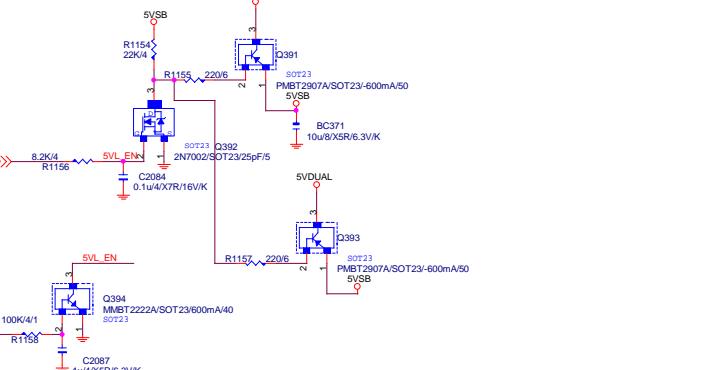
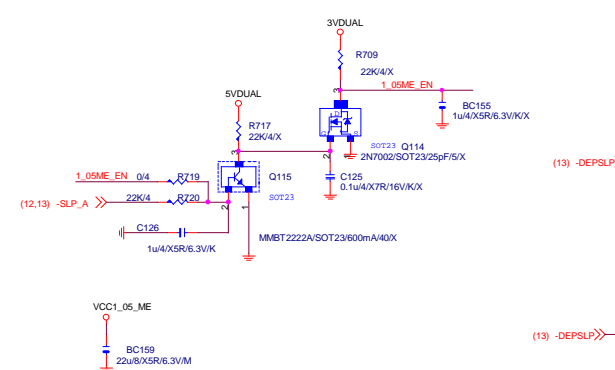
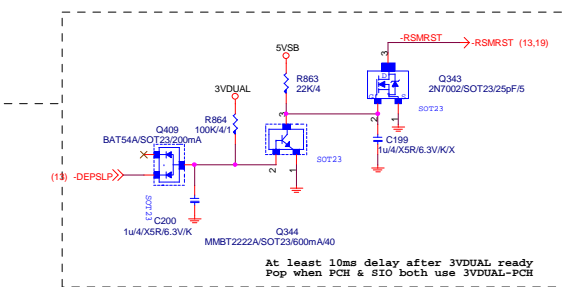
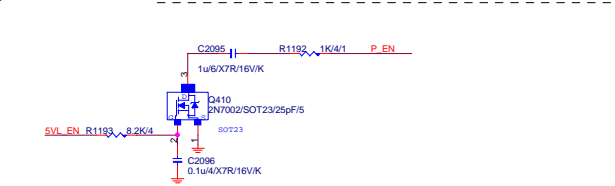
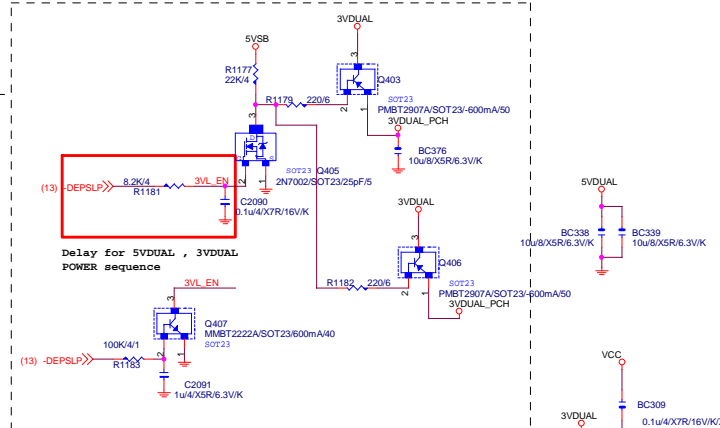
Title		
DDR POWER		
Size	Document Number	Rev
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CPU_VTT

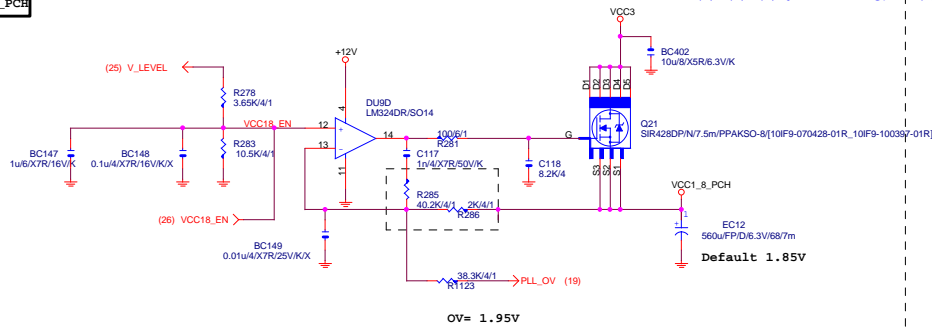


VCC_SA



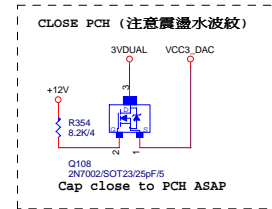


VCC1_8_PCH

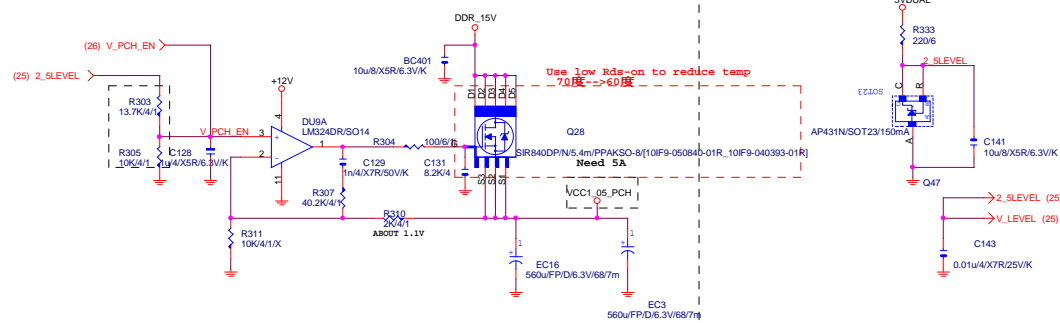


VCC3_DAC

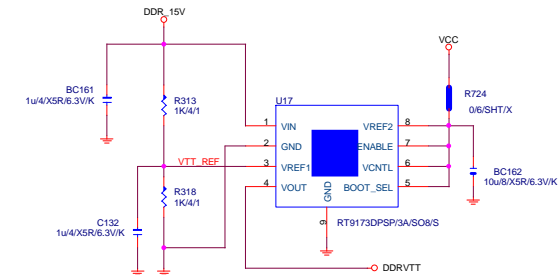
(3.3V/70mA+360uA)

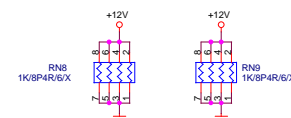
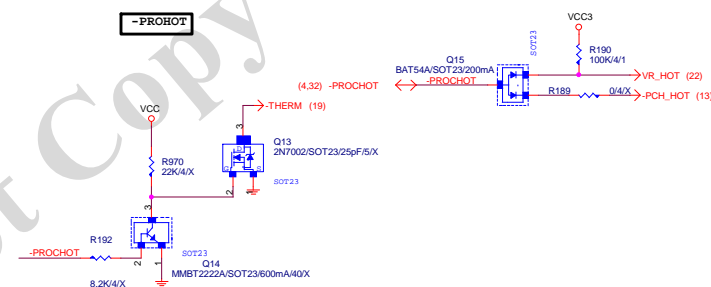
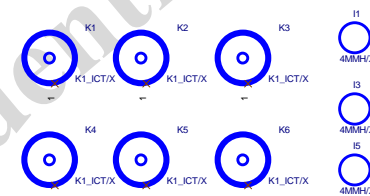
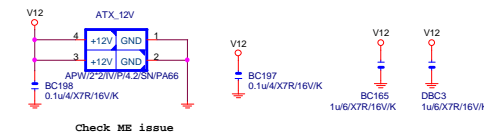


VCC1_05_PCH

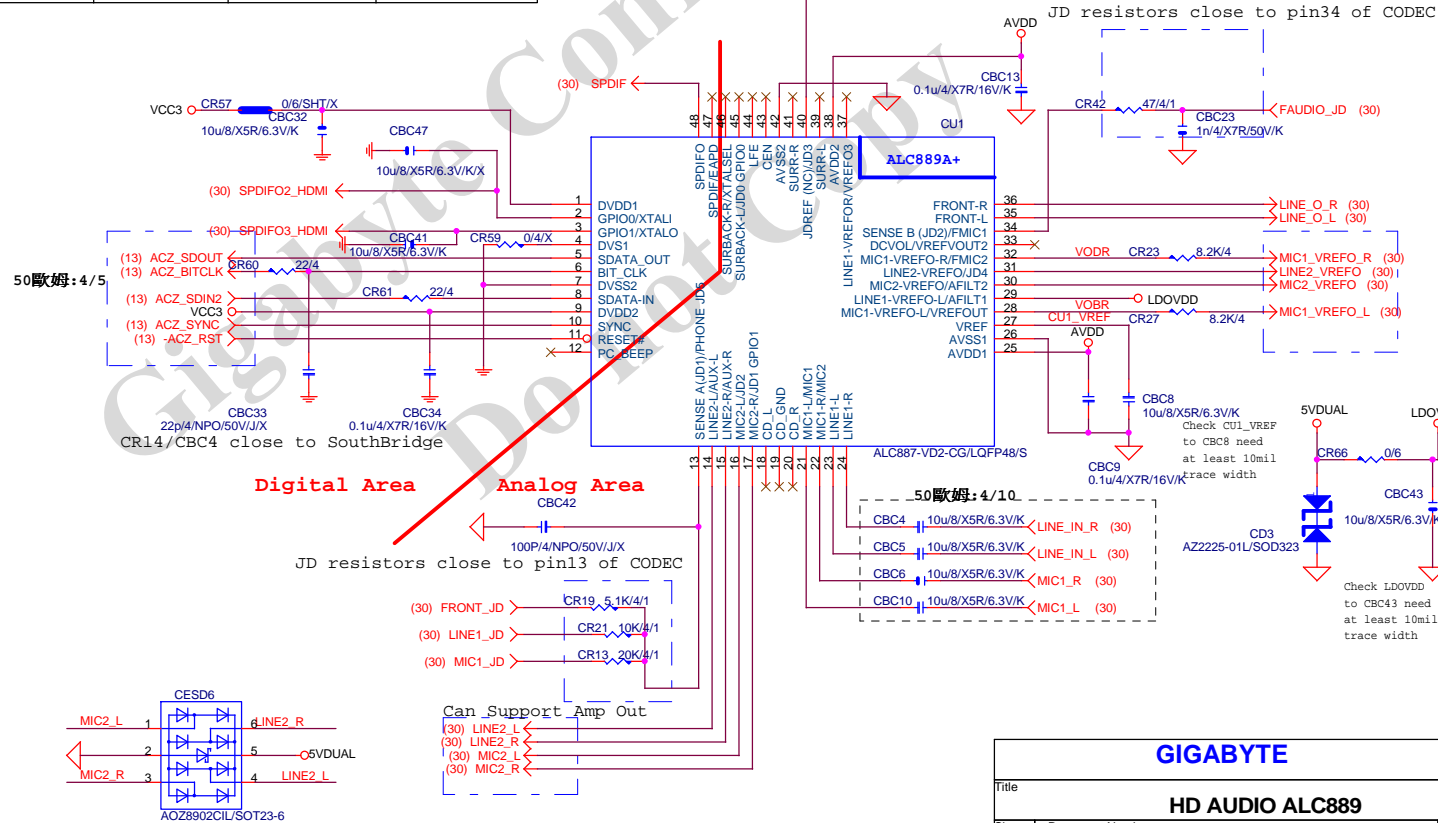


DDRVTT





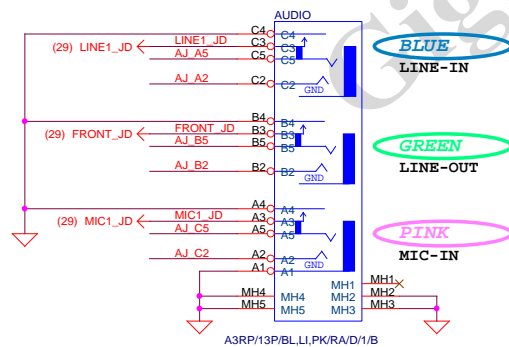
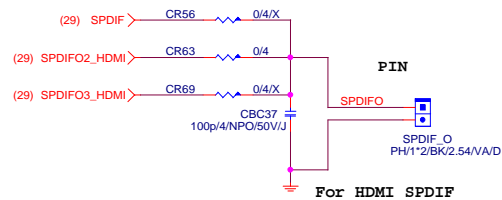
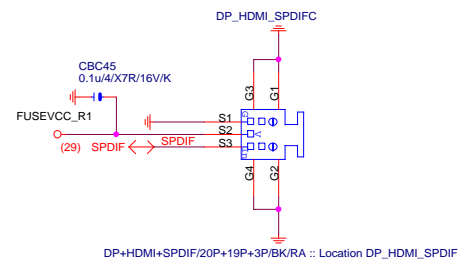
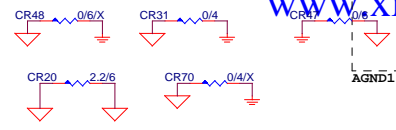
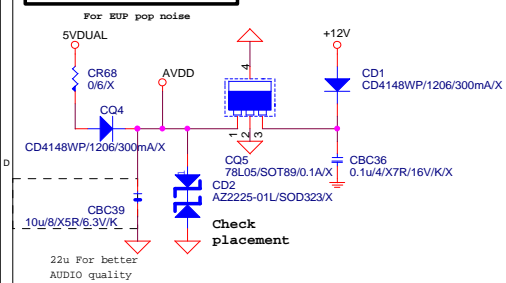
	ALC662	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR59	X	X	O	O	X
CR	X	X	X	X	0.1u/4
CBC41	O	O	X	X	O
CR42/CBC23	47ohm+1nF	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR63	X	O	O	O	O
CR56	O	X	X	X	X
CBC4/CBC5	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R
CR19	5.11K/4/1	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CR34	20K/4/1	20K/4/1	20K/4/1	5.1K/4/1	20K/4/1
CBC42/CBC46	N/A	N/A	N/A	100P/4	100P/4
CR14/CR33/CR28/CR45/ CR41/CR46/CR2/CR4/ CR35/CR39	22K/4	22K/4	22K/4	10K/4	10K/4
CR32/CR15/CR51/CR25/ CR52/CR40/CR3/CR1/ CR9/CR6/CR36/CR38	62 ohm	62 ohm	62 ohm	75 ohm	75 ohm
CR66/CD3/CBC43	O	O	X	X	O
CD1/CD2/CQ4/CQ5/CBC36	X	X	O	O	X
CR12/CR17/CR22/CR26	62 ohm	62 ohm	62 ohm	75 ohm	1K ohm



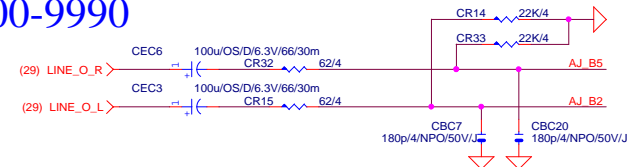
GIGABYTE

Title			HD AUDIO ALC889
Size	Document Number	ST4265-BI	
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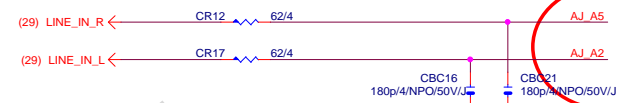
CODEC POWER/EMI PAD



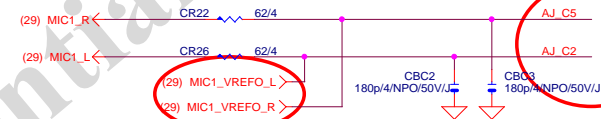
LINE-OUT



LINE-IN



MIC-IN

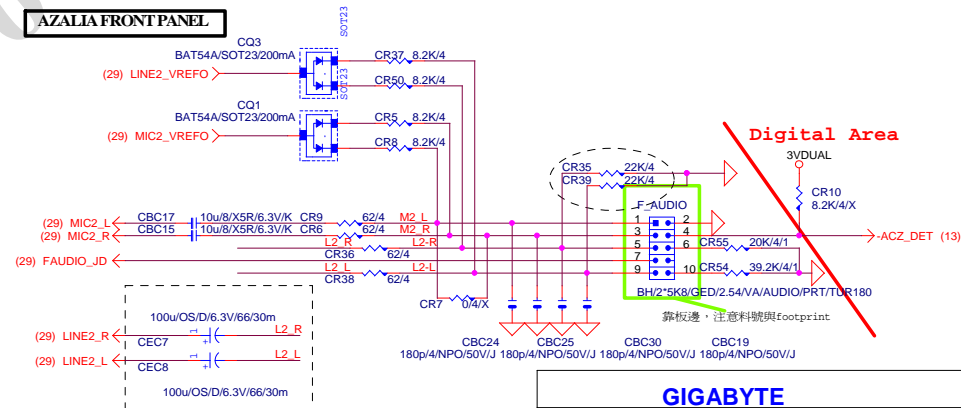


SURROUND

CEN/LFE

SURRBACK

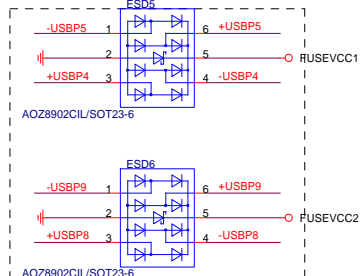
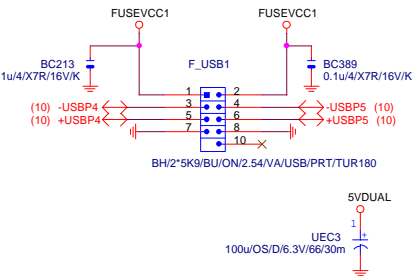
AZALIA FRONT PANEL



GIGABYTE

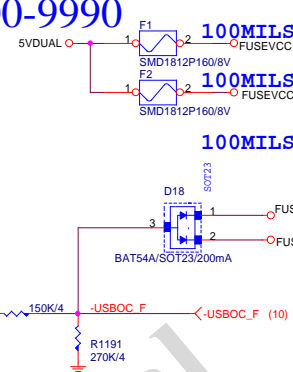
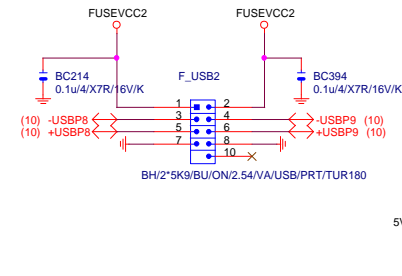
Title				Rev
AUDIO JACK				
Size Custom	Document Number			1.0
	ST4265-BI			
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FRONT USB1

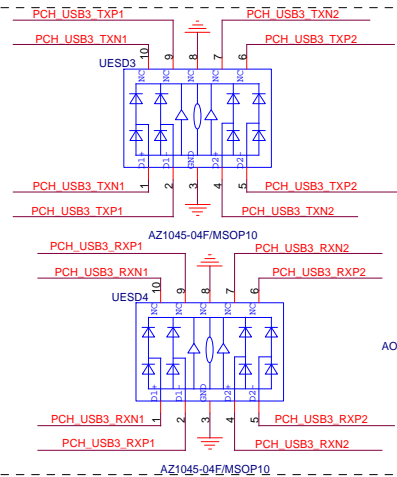
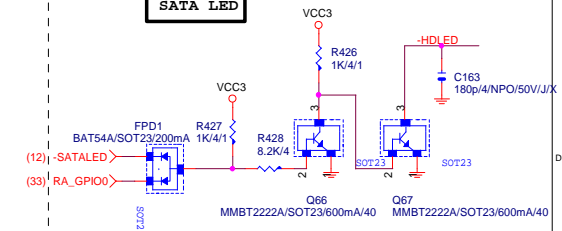


Close to connector

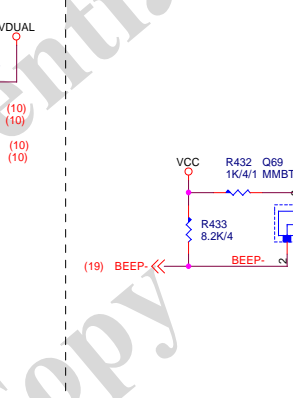
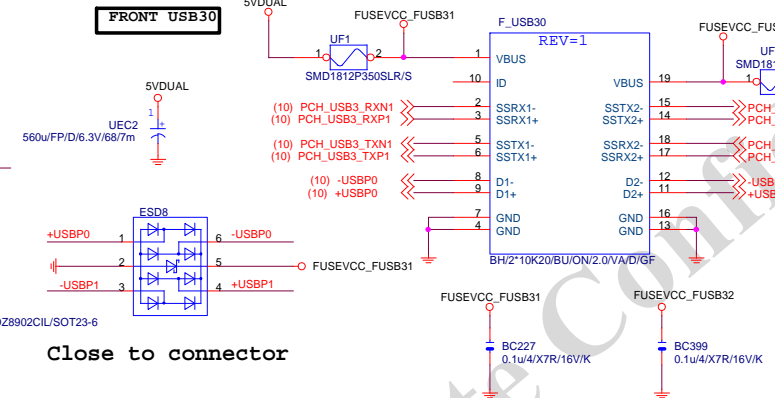
www.xinxunwei.com 400-800-9990



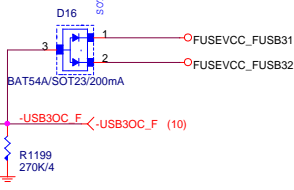
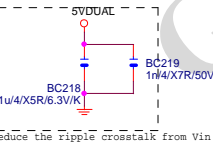
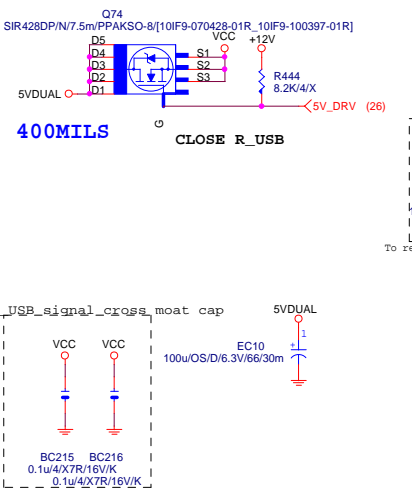
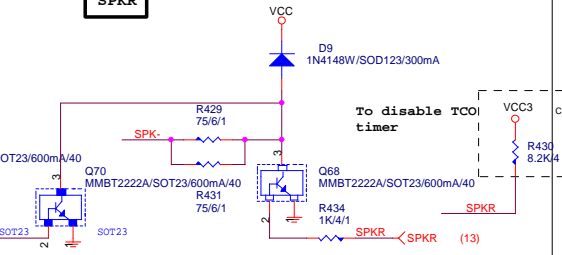
SATA LED



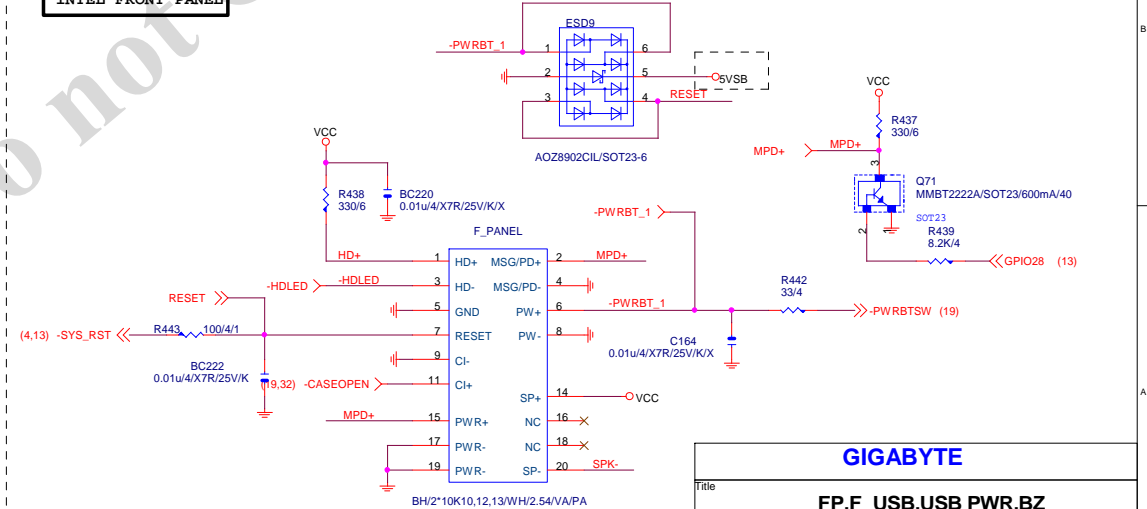
Close to connector



SPKR



INTEL FRONT PANEL



GIGABYTE

Title			FF,F_USB,USB PWR,BZ
Size			ST4265-BI
Date			Wednesday, May 30, 2012
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Rev			1.0

(19) VREF ←

(19) SYS_TEMP ←

(19) VRM_TEMP ←

(19) TEMP3 ←

C166
1u/4/X5R/6.3V/K

C167
1u/4/X5R/6.3V/K

RS4
10K/1/4/S

RS5
10K/1/4/S

C225
1u/4/X5R/6.3V/K

R446
10K/4/1

R447
10K/4/1

R448
10K/4/1

Close SIO

Close VRM

CASE OPEN

Q77 enable -CI by PCH for AMT

R1027
0/4

INTRUDER (13)

R469
1M/4

(13,14,19) RTCVDD

-CASEOPEN

-CASEOPEN (19,31)

C170
0.01u/4/X7R/25V/K

Change to 0.01u from 1u to fix the first battery on Case open abnormal.

Case Open Circuits

VOLTAGE-- H/W MONITOR

(19) VIN0

CPU_VTT

R1134 8.2K/4

C2081 1u/4/X5R/6.3V/K

VCORE

R481 8.2K/4

DDR_15V

R482 8.2K/4

VCC3

R483 6.49K/4/1

+12V

R484 75K/4/1

VCCSA

R485 8.2K/4

VCC

R486 15K/4/1

VIN5

VIN6

VIN1

VIN2

VIN4

VIN3

C201 1u/4/X5R/6.3V/K

C202 1u/4/X5R/6.3V/K

C203 1u/4/X5R/6.3V/K

C204 1u/4/X5R/6.3V/K

R879 100K/4/1

R496 15K/4/1

C205 1u/4/X5R/6.3V/K

C173 1u/4/X5R/6.3V/K

R878 10K/4/1

[illegible]

The schematic diagram illustrates the power supply for the CPU_FAN. A 12V source is connected to a network of resistors and capacitors. The output is labeled FAN101 (19). The components and their values are as follows:

- Resistors:**
 - R1138: 0/4
 - R1139: 3.3K/4/1
 - R1141: 15K/4/1
 - R1143: 6.2K/4/1
- Capacitors:**
 - BC369: 1u6/X7R/16V/K
 - C2082: 0.047u/4/X7R/16V/K

The output is connected to the CPU_FAN, which is a FAN1*4/WH/A3/PA66.

RS2 CLOSE CPU VR MOSFET

deasserted at 116 degree

+12V

DAR77 10K/4/1

DAR78 2.32K/4/1

DAR75 10K/4/1

DAR74 100K/1/4/S

DAR81 1K/4/1

DAR80 100K/1/4/S

TSM 1

TSM 2

TSM 3

DQ101 2N7002/SOT23/25pF/5

SOT23

-PROCHOT → -PROCHOT (4,28)

U1B LM358DR/SO8

R? CLOSE Q32

DAC31 0.1u/4/X7R/16V/K

BC368 0.1u/4/X7R/16V/K

U1A

3

2

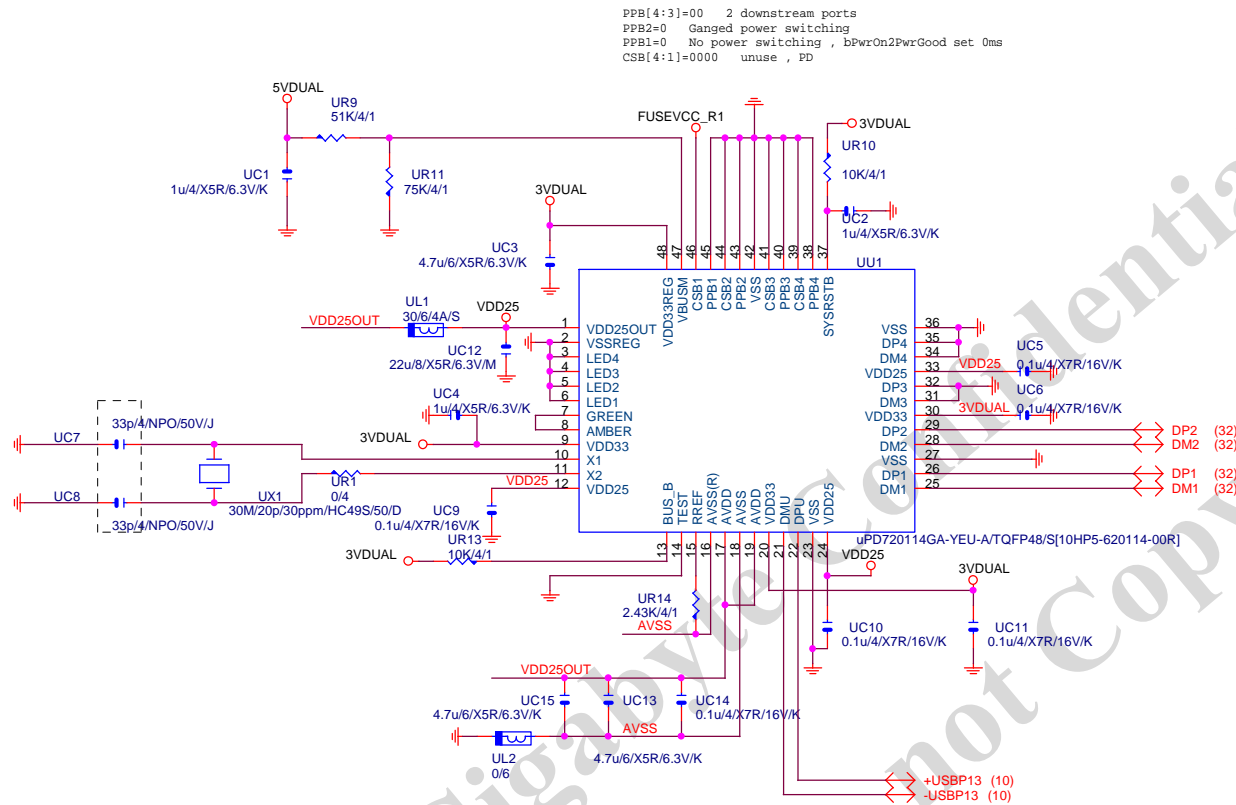
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CLOSE PWM HOT MOSFET

deasserted at 116 degree

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